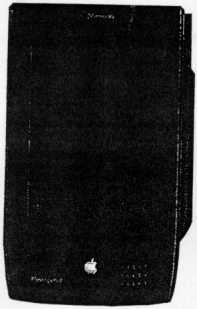
SHARP SERVICE MANUAL

CODE: 00Z



MODEL BO-A300

CONTENTS

Parts marked with "⚠" is important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

SHARP CORPORATION

CHAPTER 1. HARDWARE SPECIFICATIONS

1. CPU

Processor:	ARM610, 32-bit RISC
Clock Speed:	20MHz (Original oscillation: 40MHz)

2. Display

Resolution:	336 × 240
Display Size:	100.77 × 71.97 mm (3.96" × 2.83")

3. Storage

3-1. RAM

Capacity:	640 KB
User Area:	Approx. 190 KB (Pending)

3-2. ROM

Capacity:	4MB

4. Interface

4-1. Infrared (IR) Interface

Communication Scheme:	One-way communication
Transmission Rate:	19,200 bps (Max.)
Communication Range:	8 cm ~ 80 cm

4-2. RS-422

Communication Rate:	Up to 2M bps (Software programmable)
Connector:	8-pin mini-DIN connector

4-3. Speaker

Frequency Range:	1 KHz ~ 10 KHz
Volume:	Software Control 4 steps + None

5. Stylus Pen

No Cable, No switch

6. IC Card Slot

Interface:	68 Pin PCMCIA 2.0 (Type1 or 2)
Number of slots:	1 slot

7. CMOS Memory Backup Battery

Battery Type:	CR2032 × 1
Output:	3 VDC
Battery Life:	100 days after exhaustion of main battery (Pending)

8. Power Supply

8-1. Internal Battery

Battery Type:	AlMn (AAA × 4) or Ni-Cd Battery Pack (Option)
Output:	6VDC
Battery Life:	1.4 Watt (Pending)

8-2. AC Adapter (Option)

Input:	100 to 240 V
Output:	7 VDC, 500 mA

9. Size

9-1. Dimensions

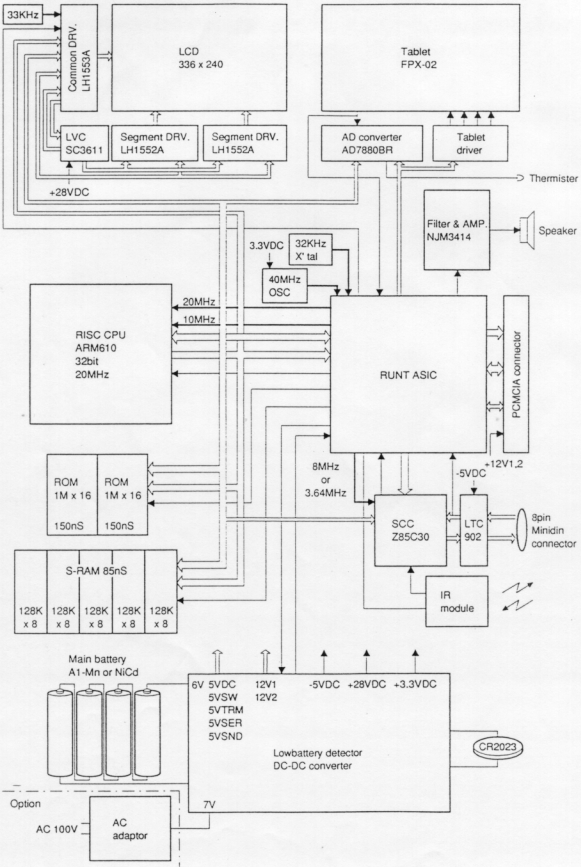
Height:	27.8 mm (1.09"); without feet
Width:	111.5 mm (4.39")
Depth:	181.5 mm (7.15")
Stylus Pen:	125.7 × 8.5 × 5.5 mm (4.95" × 0.33" × 0.22")

9-2. Weight

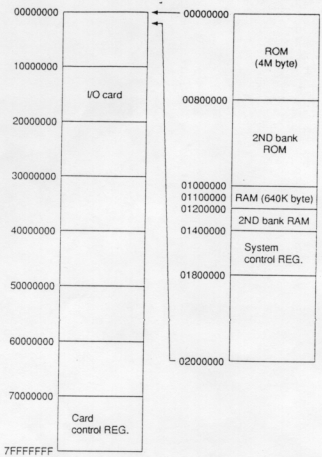
Approx. 440 g (including battery)

CHAPTER 2. HARDWARE DESCRIPTION

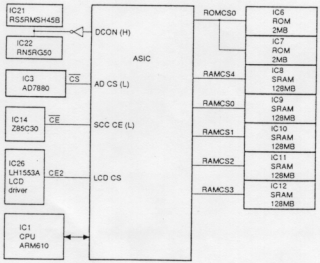
1. Block diagram



2. Memory map explanation

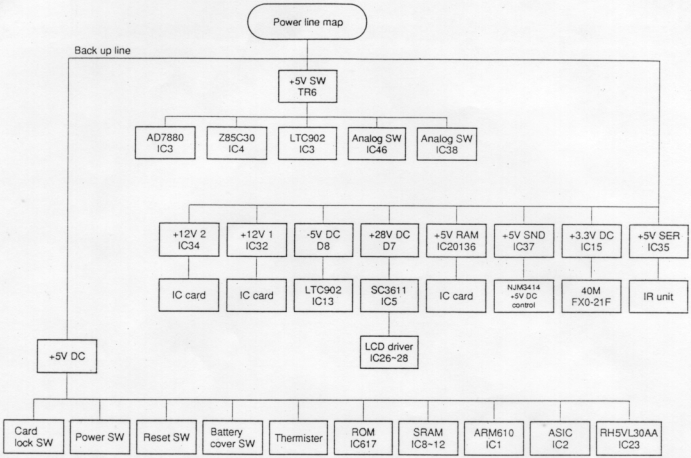


3. Chip select and related explanation



ASIC: APPLICATION
SPECIFIC
INTEGRATED
CIRCUIT

4. Power system diagram



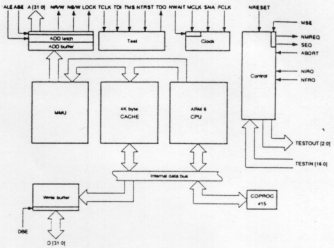
5. LC, LSI description

① ARM610 (CPU) description

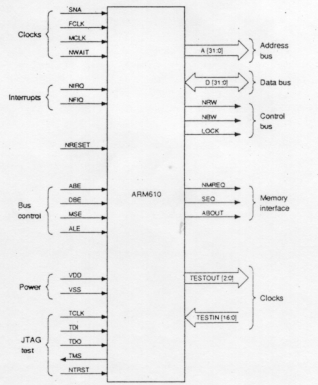
The ARM610 (CPU) is a 32-bit RISC microprocessor which is equipped with an MMU (Memory Management Unit) and a 4KB cash memory.
The ARM has input clocks FCLK and MCLK. MCLK signal is used in the memory cycle of the ARM. In making access to the RAM or the ROM, the access speed is at a high level in order to reduce the difference in the access speed of the ARM. So the ARM must be weighted. In this case, however, the ARM is not directly weighted, but MCLK signal is extended via ASIC and memory access is performed.
The FCLK's 40MHz clock is divided into 20MHz by ASIC.
20MHz ARM system clock ??????????????????

NAME	PIN	I/O	DESCRIPTION	
A (31:0)		O	Address bus	Address bus
ABE	74	I	Address bus enable	Bus Controls
ABORT	138	I	External abort	Memory Interface
NBW	72	O	Not byte/word WORD/BYTE selection	Control Bus
D (31:0)		I/O	Data bus	Data bus
DBE	4	I	data bus enable	Bus Controls
FCLK	139	I	Fast clock input	CLOCKS
NFIQ	131	I	Not fast interrupt request.	Interrupts
NIRQ	132	I	Not interrupt request.	Interrupts
LOCK	73	O	Locked operation.	Control Bus
MCLK	140	I	Memory clock input.	CLOCKS
NMREQ	2	O	Not memory request.	Memory Interface
MSE	1	I	Memory request/ Sequential enable	Bus Controls
ALE	117	I	Address latch enable.	Bus Controls
NRESET	137	I	Not reset.	Control Bus
NRW	71	O	Not read/write	Control Bus
SEQ	3	O	Sequential address	Memory Interface
SNA	144	I	Synchronous/not Asynchronous.	CLOCKS
NTEST	13	I	Not test.	DEVICE TEST
TCLK	53	I	Test interface reference clock	DEVICE TEST
TDI	49	I	Test interface data input.	DEVICE TEST
TDO	48	O	Test interface data output.	DEVICE TEST
TMS	52	I	Test interface mode select	DEVICE TEST
NTRST	50	I	Test interface reset.	DEVICE TEST
NWAIT	143	I	Not wait.	CLOCKS
VDD		I	Positive Supply	POWER
VSS		I	Ground Supply	GND
TESTOUT		O	Test bus output	CHIP TEST
TESTIN		I	Test bus input	CHIP TEST

①-1 Block Diagram (ARM 610)



Functional Diagram



② ASIC (Application Specific Integrated Circuit) description

The ASIC used in Junior-1 has the following functions:

1. The ARM 610 (CPU) bus control (ARM bus glue logic)
2. Memory control
3. PCMCIA parallel I/O bus
4. SCC control
   Serial port control, Communication support with a Mackintosh serial port, IR communication control
5. Power management system
6. LCD display control
7. Tablet control
8. Sound generation
9. Clock function

⁎ Power management

(Start) There are following three conditions for starting operations from the standby state.
(1) 32.768KHz is oscillating.
(2) Batt-fault is HIGH.
(3) VCC-Fault turns HIGH within the specified time.
When the reset or ON-SW is inputted under the above conditions, DC-ON becomes HIGH to start the convertor. When it will not operate with the reset OK, check the above three conditions.

(Stop) The system is normally stopped by the software. In case of emergency, however, it is shut down by ASIC.
There are two conditions for the emergency shut down.
1. VCC-Fault is LOW.
2. Batt-Fault is LOW.
When either of the above two occurs, ASIC stops CLK to ARM and fixes the data bus to LOW. To continue the operation when the system returns rom the above conditions, ARM, ASIC, RAM and ROM are connected to the backup system power source.

⁎ Clock adjustment (Advance adjustment)

Advance adjustment

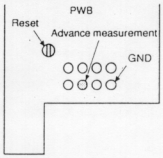
Used jig/meter
Advance meter (Made by Sansei electronics, Model SS-406 + Frequency divider)
Sensor (Contact-type)

Temperature	min.	max.	Center value (reference)
15°C	−0.30	−0.20	−0.25
16°C	−0.28	−0.12	−0.20
17°C	−0.26	−0.04	−0.15
18°C	−0.24	+0.04	−0.10
19°C	−0.22	+0.12	−0.05
20 ~ 30 °C	−0.15	+0.15	±0.00

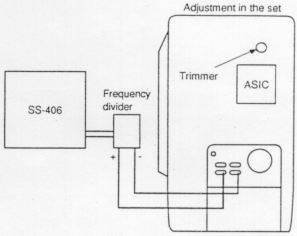
(sec/day)

⁎ Adjust according to the reference in the table.

Measurement pad position



⁎ For the adjustment, use a screwdriver.



②-1 Pin Assignments & Signal Descriptions (ASIC)

This appendix lists the signals assigned to each RUNT pin and provides a brief description of each of those signals.

Pin No.	Pin Name	I/O	Active	Signal Description
1	TDI	I	High	jtag serial data in
2	VDD3			
3	GEN_RD_L	O	Low	read signal to a/d converter and sec
4	GEN_WR_L	O	Low	write signal to a/d converter, scc and lcd
5	SCC_A_B	O	High	scc channel a/b select
6	SCC_CE_L	O	Low	scc chip enable
7	SCC_D_C	O	High	scc data/control select
8	RTXCLK	O	High	scc bus clock 3.6364mhz, or 8Mhz
9	SCCWREQA_L	I	Low	scc channel a dma write request
10	SCCWREQB_L	I	Low	scc channel b dma write request
11	SIO_L	I	Low	scc interrupt
12	SCC_TXDB	I	High	pre modulated ir data stream from scc
13	IR_TXD_L	O	Low	modulated ir data stream to ir module
14	SCCDTRREQA_L	I	Low	scc channel a dma read request
15	SCCDTRREQB_L	I	Low	scc channel b dma read request
16	ADIQ	I	Hight	a/d interrupt
17	VDD			
18	AD_VREF_ON_L	O	Low	a/d enable voltage reference
19	AD_CS_L	O	Low	a/d chip enable
20	AD_CKI	O	High	a/d clock signal 2.0 mhz
21	GPI	I	High	External system wakeup, serial GPI signal
22	TAB_SWX_L	O	Low	Turn on X sampling drive, avtive low
23	TAB_SWX	O	High	Turn on X sampling drive, active high
24	GND2			
25	TAB_SWY_L	O	Low	Turn on Y sampling drive, avtive low
26	TAB_SWY	O	High	Turn on Y sampling drive, active high
27	TAB_MON	O	High	Set up tablet for threshold measurements
28	TAB_XMON_L	O	Low	Set up tablet for threshold measurements
29	TAB_YMON_L	O	Low	Set up tablet for threshold measurements

Pin No.	Pin Name	I/O	Active	Signal Description
30	TABIQ	I	High	tablet interrupt
31	LCD_LVC_ON	O	High	Enable bias voltage generator
32	LCD_CS	O	High	lcd chip enable
33	GND			
34	LCD_CLK	O	High	3.3Mhz clock for LCD operations
35	LCD_BUSY	I	High	lcd busy (operation in progress)
36	LCD_DC_CLK	O	High	32.768Khz clock for PWM for +24V, –5V
37	PWM	O	High	pwm output to integrator
38	VOL0	O	High	sound out volume control 0
39	VOL1	O	High	sound out volume control 1
40	POWERMAIN	O	High	enable main power supply
41	NICAD_IN	I	High	nicad batteries are installed
42	VCCFAULT_L	I	Low	vcc not within regulation
43	SAMP_TEMP	O	High	connect temperature sensor to a/d converter
44	SAMP_BACK	O	High	connect lithium battery to a/d converter
45	GND3			
46	SAMP_MAIN	O	High	connect main battery to a/d converter
47	SAMP_TAB	O	High	connect tablet to a/d converter
48	SYSRESET_L	I	Low	system reset switch
49	SYSPOWER_L	I	Low	system power on button
50	CARDLOCK_L	I	Low	card lock switch disengaged
51	BATCOV_L	I	Low	battery cover opened
52	BFAULT_L	I	Low	main battery failure or disconnected
53	X5VTRIM_ON	O	High	enable card +5V supply
54	X5VSERIAL_ON	O	High	enable scc, driver and IR supply
55	X5VSOUND_ON	O	High	enable sound out supply
56	X12V_CONT_1	O	High	enable voltage vpp1, from +5VTRM to +12V
57	X12V_CONT_2	O	High	enable voltage vpp2, from +5VTRM to +12V
58	PCMCIA0CD2_L	O	Low	card detect 2
59	VDD			
60	WP/IOIS16*	IO	Low	write protect/io port is 16 bits
61	PCMCIADATA10	IO	High	data bus

Pin No.	Pin Name	I/O	Active	Signal Description
62	PCMCIADATA2	IO	High	data bus
63	GND2			
64	JTCLK	I	High	jtag test clock
65	TRST_L	I	Low	jtag state machine reset
66	PCMCIADATA1	IO	High	data bus
67	bvd1/statusChg	I	Low	battery voltage 1/ status change
68	GND			
69	PCMCIADATA0	IO	High	data bus
70	PCMCIADATA9	IO	High	data bus
71	PCMCIAADR0	IO	High	address bus
72	BVD2/SPKR	I	Low	battery voltage 2/ speaker (not supported)
73	PCMCIADATA8	IO	High	data bus
74	VDD			
75	PCMCIAADR1	IO	High	address bus
76	REG_L	O	Low	register memory select
77	PCMCIAADR2	IO	High	address bus
78	PCMCIAINPACK_L	I	Low	input access valid
79	PCMCIAADR3	IO	High	address bus
80	GND3			
81	PCMCIAWAIT_L	I	Low	wait cycle indicator
82	PCMCIAADR4	IO	High	address bus
83	RESET	O	High	card reset
84	GND2			
85	PCMCIAADR5	IO	High	address bus
86	PCMCIAADR6	IO	High	address bus
87	GND			
88	PCMCIAADR25	O	Low	address bus
89	PCMCIAADR7	IO	High	address bus
90	PCMCIAADR24	IO	High	address bus
91	PCMCIAADR12	IO	High	address bus
92	VDD			
93	PCMCIAADR23	IO	High	address bus
94	PCMCIAADR15	IO	High	address bus
95	PCMCIAADR22	IO	High	address bus
96	PCMCIAADR16	IO	High	address bus
97	PCMCIAADR21	IO	High	address bus
98	GND			
99	BUSY/INTREQ_L	I	Low	card busy/card interrupt
100	PCMCIAADR20	IO	High	address bus
101	WE_PRGM_L	IO	High	write enable
102	VDD3			
103	PCMCIAADR19	IO	High	address bus
104	PCMCIAADR14	IO	High	address bus
105	PCMCIAADR18	IO	High	address bus
106	VDD			
107	PCMCIAADR13	IO	High	address bus
108	PCMCIAADR17	IO	High	address bus
109	PCMCIAADR8	IO	High	address bus
110	IO_WR_L	O	Low	io cycle write
111	PCMCIAADR9	IO	High	address bus
112	GND2			
113	IO_RD_L	O	Low	io cycle read
114	PCMCIAADR11	IO	High	address bus
115	CE2_L	O	Low	card enable 2 (MSB)

Pin No.	Pin Name	I/O	Active	Signal Description
116	PCMCIAADR10	IO	High	address bus
117	PCMCIADATA15	IO	High	data bus
118	GND			
119	CE1_L	O	Low	card enable 1 (LSB)
120	PCMCIADATA14	IO	High	data bus
121	PCMCIADATA7	IO	High	data bus
122	PCMCIADATA13	IO	High	data bus
123	PCMCIADATA6	IO	High	data bus
124	VDD			
125	PCMCIADATA12	IO	High	data bus
126	PCMCIADATA5	IO	High	data bus
127	PCMCIADATA11	IO	Low	data bus
128	TMS	I	High	jtag control input
129	TDO	O	High	jtag serial data out
130	PCMCIADATA4	IO	High	data bus
131	PCMCIADATA3	IO	High	data bus
132	PCMCIAOCD1_L	I	Low	card detect 1
133	PCMCIAOE_L	O	Low	output enable
134	RAMCS[7]	O	High	"ram chip select, bank1, byte0, D<31..24>"
135	RAMCS[6]	O	High	"ram chip select, bank1, byte1, D<23..16>"
136	RAMCS[5]	O	High	"ram chip select, bank1, byte2, D<15..8>"
137	RAMCS[4]	O	High	"ram chip select, bank1, byte3, D<7..0>"
138	RAMCS[3]	O	High	"ram chip select, bank0, byte0, D<31..24>"
139	RAMCS[2]	O	High	"ram chip select, bank0, byte1, D<23..16>"
140	RAMCS[1]	O	High	"ram chip select, bank0, byte2, D<15..8>"
141	RAMCS[0]	O	High	"ram chip select, bank0, byte3, D<7..0>"
142	GND			
143	OSC32KIN	I	High	32khz crystal connection
144	OSC32KOUT	O	High	32khz crystal connection
145	OSC40MIN	I	High	40mhz clock input
146	GND			
147	RAMWE_L	O	Low	ram write enable
148	RAMOE_L[3]	O	Low	"ram output enable, byte0, D<31..24>"
149	RAMOE_L[2]	O	Low	"ram output enable, byte1, D<23..16>"
150	RAMOE_L[1]	O	Low	"ram output enable, byte2, D<15..8>"
151	RAMOE_L[0]	O	Low	"ram output enable, byte3, D<7..0>"
152	GND2			

Pin No.	Pin Name	I/O	Active	Signal Description
153	ADDR[31]	IO	High	address bus
154	ADDR[30]	IO	High	address bus
155	VDD			
156	ADDR[29]	IO	High	address bus
157	ADDR[28]	IO	High	address bus
158	ADDR[27]	IO	High	address bus
159	GND3			
160	ADDR[26]	IO	High	address bus
161	ADDR[25]	IO	High	address bus
162	VDD3			
163	ADDR[24]	IO	High	address bus
164	GND			
165	ADDR[23]	IO	High	address bus
166	ADDR[22]	IO	High	address bus
167	ADDR[21]	IO	High	address bus
168	ADDR[20]	IO	High	address bus
169	ADDR[19]	IO	High	address bus
170	VDD			
171	ADDR[18]	IO	High	address bus
172	ADDR[17]	IO	High	address bus
173	ADDR[16]	IO	High	address bus
174	ADDR[15]	IO	High	address bus
175	ADDR[14]	IO	High	address bus
176	GND2			
177	GND			
178	ADDR[13]	IO	High	address bus
179	ADDR[12]	IO	High	address bus
180	ADDR[11]	IO	High	address bus
181	ADDR[10]	IO	High	address bus
182	ADDR[9]	IO	High	address bus
183	ADDR[8]	IO	High	address bus
184	ADDR[7]	IO	High	address bus
185	VDD			
186	ADDR[6]	IO	High	address bus
187	ADDR[5]	IO	High	address bus
188	ADDR[4]	IO	High	address bus
189	GND			
190	ADDR[3]	IO	High	address bus
191	ADDR[2]	IO	High	address bus
192	LSITEST_PO	O	High	lsi test output
193	LSITEST_TN	I	Low	lsi test input (tri-state all pins)
194	GND			
195	ADDR[1]	IO	High	address bus
196	ADDR[0]	IO	High	address bus
197	DATA[31]	IO	High	data bus
198	GND2			
199	DATA[30]	IO	High	data bus
200	DATA[29]	IO	High	data bus
201	GND			
202	DATA[28]	IO	High	data bus
203	DATA[27]	IO	High	data bus
204	DATA[26]	IO	High	data bus
205	DATA[25]	IO	High	data bus
206	VDD			
207	DATA[24]	IO	High	data bus
208	DATA[23]	IO	High	data bus
209	DATA[22]	IO	High	data bus
210	DATA[21]	IO	High	data bus
211	GND			
212	DATA[20]	IO	High	data bus

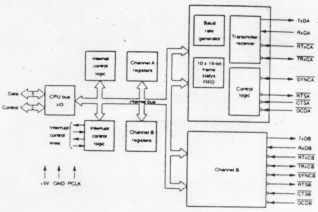
Pin No.	Pin Name	I/O	Active	Signal Description
213	DATA[19]	IO	High	data bus
214	DATA[18]	IO	High	data bus
215	DATA[17]	IO	High	data bus
216	DATA[16]	IO	High	data bus
217	VDD			
218	DATA[15]	IO	High	data bus
219	DATA[14]	IO	High	data bus
220	DATA[13]	IO	High	data bus
221	DATA[12]	IO	High	data bus
222	DATA[11]	IO	High	data bus
223	GND			
224	DATA[10]	IO	High	data bus
225	DATA[9]	IO	High	data bus
226	GND2			
227	DATA[8]	IO	High	data bus
228	DATA[7]	IO	High	data bus
229	DATA[6]	IO	High	data bus
230	VDD			
231	DATA[5]	IO	High	data bus
232	DATA[4]	IO	High	data bus
233	DATA[3]	IO	High	data bus
234	DATA[2]	IO	High	data bus
235	GND			
236	DATA[1]	IO	High	data bus
237	DATA[0]	IO	High	data bus
238	VDD3			
239	ROMCS_L[1]	O	Low	*rom chip select and output enable, bank1*
240	ROMCS_L[0]	O	Low	*rom chip select and output enable, bank0*
241	FCLK	O	High	*arm processor clock, 20mhz*
242	MCLK	O	High	*arm bus interface clock, 10mhz*
243	IRQ_L	O	Low	arm normal priority interrupt
244	GND3			
245	FIQ_L	O	Low	arm high priority interrupt
246	RESET_L	O	Low	arm reset
247	ALE	O	High	arm address latch enable
248	VDD			
249	BE	O	High	arm bus and control signal enable
250	R_L_W	IO	High	arm read/write indication (active low read)
251	B_L_W	IO	High	arm byte/word indication (active low byte)
252	LOCK	IO	High	arm interlocked bus transaction
253	MREQ_L	I	Low	arm memory request indication
254	ABORT	O	High	arm illegal access abort
255	AD_CONV_L	O	Low	a/d converter conversion start
256	GND			

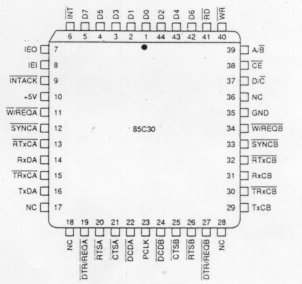
③ Z85C30 description

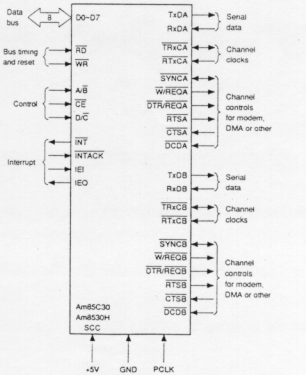
The Z85C30 is called Serial Communication Controller (SCC) and is equipped with 2-channel port.
In Junior-1, channel A controls RS422 serial port and channel B controls 1R unit.
ASIC has four DMA's for SCC channel A and B (??????????????????), and data transmission is enabled between SCC and ASIC and memory without going through the CPU.

Name	Pin	I/O	Description	
RD	41	I	READ	Bus timing and reset
WR	40	I	WRITE	Bus timing and reset
RTXCA	13	I	RECEIVE/TRANSMIT CLOCK A	Channel clock
RTXCB	32	I	RECEIVE/TRANSMIT CLOCK B	Channel clock
TRXCA	15	I/O	TRANSMIT/RECEIVE CLOCK A	Channel clock
TRXCB	30	I/O	TRANSMIT/RECEIVE CLOCK B	Channel clock
CTSA	21	I	CLEAR TO SEND A	channel control
CTSB	25	I	CLEAR TO SEND A	channel control
DCDA	22	I	DATA CARRIER DETECT A	channel control
DCDB	24	I	DATA CARRIER DETECT A	channel control
DREQA	19	O	DATA TERMINAL READY/REQUEST A	channel control
DREQB	27	O	DATA TERMINAL READY/REQUEST B	channel control
RTSA	20	O	REQUEST TO SEND A	channel control
RTSB	26	O	REQUEST TO SEND B	channel control
SYNCA	12	I/O	SYNCHRONIZATION A	channel control
SYNCB	33	I/O	SYNCHRONIZATION B	channel control
WREQA	11	O	WAIT REQUEST A	channel control
WREQB	34	O	WAIT REQUEST B	channel control
A/B	39	I	CHANNEL A/CHANNEL B SELECT	Control
CE	38	I	CHIP ENABLE	Control
D/C	37	I	DATA/CONTROL SELECT	Control
D (7:0)		I/O	DATA BUS	Data bus
IEI	7	I	INTERRUPT ENABLE IN	Interrupt
IEO	8	O	INTERRUPT ENABLE OUT	Interrupt
INT	6	O	INTERRUPT REQUEST	Interrupt
INTACK	9	I	INTERRUPT ACKNOWLEDGE	Interrupt
RXDA	14	I	RECEIVE DATA A	Serial data
RXDB	31	I	RECEIVE DATA B	Serial data
TXDA	16	O	TRANSMIT DATA A	Serial data
TXDB	29	O	TRANSMIT DATA B	Serial data
GND	35		GND	
PCLK	23	I	CLOCK	
+5V	10		VCC	

③-1 BLOCK DIAGRAM (Z85C30)





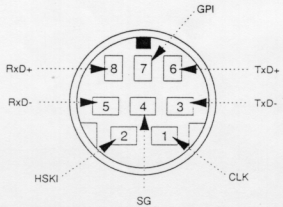


④ LTC902

The LTC902 is a driver to perform sending and receiving of TTL level serial data from SCC in the RS422 standards. Junior-1 supports Local Talk on this port.

Name	Pin	I/O	Description
TXD	1	I	TTL level different driver input
DTR	2	I	TTL level single-end inverting driver input
TXEN	3	O	TTL level differential driver output enable
SHUTD	4	I	TTL level shutdown input
RXEN	5	I	TTL level receiver input
GPI	6	O	Inverting single-ended receiver output
HSKI.R	7	O	Non-inverting single-ended receiver output
SRXDO	8	O	Differential receiver output
GND	9		GND
RXD+	10	I	Non-inverting input to differential receiver
RXD–	11	I	Inverting input to differential receiver
HSKI	12	I	Non-inverting receiver input
GPI	13	I	Inverting receiver input
Vee	14		Negative supply (–5V)
HSKO	15	O	Single-ended inverting driver output
TXD+	16	O	Non-inverting driver output
TXD–	17	O	Inverting differential driver output
VCC	18		Positive supply +5V

Serial port pin arrangement



Name	Pin	I/O	Description
CLK	1	O	RxD, TxD CLOCK
HSKI	2	I	Handshake input or external clock
TxD–	3	O	Transmitted Data (inverted)
SG	4		Signal Ground
RxD–	5	I	Received Data (inverted)
TxD+	6	I	Balanced Transmit
GPI	7	I	General-purpose input
RxD+	8	I	Balanced Receive

⑤ AD7880

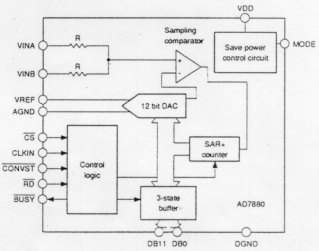
The AD7880 ia a 12-bit A/D convertor which operates on signal +5V at high speeds with low power consumption. It is composed of the 3μsec operation track/hold amplifier, the serial comparison type ADC with conversion time of 12μsec, the interface logic of multi-functions, and the input range variable circuit. It is also equipped with the power save feature.

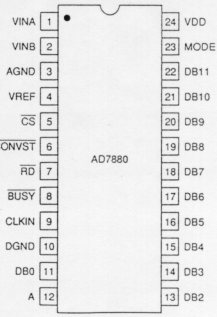
The MODE pin is used in the power save mode. The measurement range of voltage is 0 ~ +5V SW. There are five voltages which are measured with the AD convertor; the tablet X axis, the Y axis, the temperature detection (thermistor division), the main battery, and the backup battery. To select the inputs, IC25 analog SW is controlled with the ASIC control pin.

When the AD convertor does not operate properly, the following points must be checked.

CLKIN: 2MHz CLOCK
VREF: Same voltage as VDD.
MODE: Turns high when operating.
CS, RD: Operates.
IC25: Operates.

Block diagram





Pin descriptions

Pin No.	Pin name	Descriptions
1	V_{INA}	Analog input
2	V_{INB}	Analog input
3	AGND	Analog ground
4	V_{HRF}	Voltage reference input. Normally connected to V????.
5	$\overline{CS}$	Chip select. Active LOW logic input. When this input is LOW, this device is selected.
6	$\overline{CONVST}$	Conversion start. When this input is switched from LOW to HIGH, the track hold goes into the hold mode, starting conversion. CONVST input is asynchronous with CLKIN, and independent from CS and RD.
7	$\overline{RD}$	Read. Active LOW logic input. This input is used to enable the data output when CS becomes LOW.
8	$\overline{BUSY}$	Active LOW logic output. This signal indicates the convertor state. BUSY becomes LOW during conversion.
9	CLKIN	Clock input. TTL-compatible logic input. Used as the clock signal source for the A/D convertor. The mark/space ratio of this clock signal is in the range of 40/60 ~ 60/40.
10	DGND	Digital ground
11~22	DB0~DB11	3-state data output. When CS and RD become LOW at the same time, this signal becomes active.
23	MODE	MODE input. Used to set the device to the power save mode. (When MODE=0V, the power save mode.) At logic HIGH (MODE=V??), normal operations.
24	V_{DD}	Power voltage. Rated value +5V.

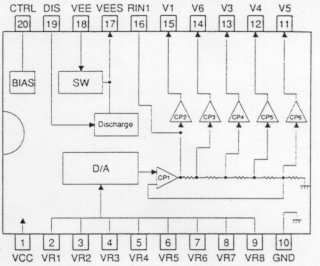
⑥ LVC (SC3611)

1) Brief functional description

LCD driver power control

Input potentiometers, VR1~VR8, perform D/A conversion to set up output voltages V1, V3~V6 that controlled by VCC input line and on and off of the VEES output.

2) Block diagram

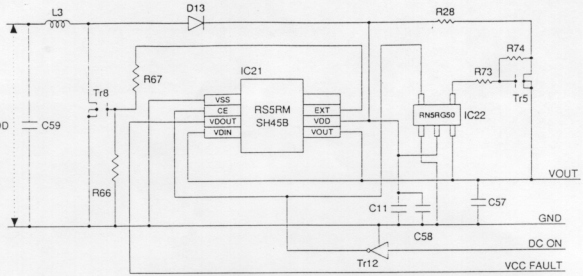


SC3611 block diagram

3) Pin description

Pin No.	Signal name	IN/OUT	Description
2~9	VR1~VR8	IN	As an 8-bit digital value is set with VR1 set to SB and VR8 to MSB, the LCD drive voltage is controlled. (Control input)
11~15	V1, V3~V6	OUT	$V3=\frac{12}{13}V1$, $V4=\frac{11}{13}V1$, $V6=\frac{1}{13}V$ (LCD power supply line)
20	CTRL	—	Using the bias current setting, the output capacity is controlled by V1, V3~V6. (Bias line)
18	VEE	IN	Source power supply to issue the LCD power supplies V1, V3~V6. (LCD power supply input)
17	VEES	OUT	VEE is produced when VCC(SW) is at a high and high impedance when VCC(SW) is at a low.
16	RIN1	IN	Same voltage as V1. It has no buffer function. (Bias line)
12	GND	—	
19	DIS	IN	Output discharge control. Not used.

6. Power circuit (5V stabilizing power)

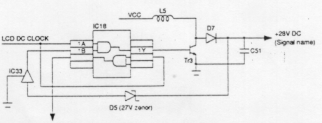


TR8: Boosting FET
TR5: Dropping FET

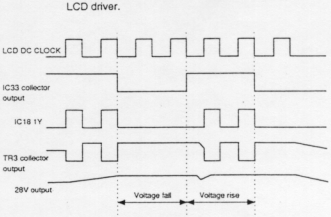
Power circuit operations (5V stabilizing power)

1. IC21 (RS5RMSH45B) has the 5.5V regulator and the external boosting DC/DC convertor control pin to control boosting FET TR8.
   IC22 (RN5RG50) controls dropping FET TR5. IC21 and IC22 chip select is performed by ASIC DC ON signal.
   IC21 chip select CE pin stops only the boosting control circuit when not active (CE = H). (Power save mode)
   Though IC21 internal regulator circuit is in standby state, the regulate voltage is outputted from VOUT.
   This voltage (VOUT) is supplied to ASIC, ARM, ROM, RAM, and LCD unit.
   When ASIC starts power ON operation, IC21 and IC22 are chip-selected to operate the boosting/dropping circuit of TR8/TR5, stabilizing the power.
2. IC21 VOUT pin output voltage is inputted to IC21 voltage detection pin VDIN. When VDIN falls below 4.5V, IC21 VDOUT supplies a low output, which is inputted to ASIC as VCC FAULT signal. Then ASIC terminates the system operation.
   When CE = H during the system operation is terminated, VDD is outputted from IC21 VOUT.
   When the input voltage rises above 5.5V, VOUT outputs the regulate output of 5.5V.
   = Note for servicing
   Since the FET used in this circuit is weak in static electricity, use great care for anti-static-electricity measures such as a grounding band when servicing.

The output voltage is controlled by zenor D5. When the output exceed the total of zenor voltage (27V) and IC33 VBE, IC33 is turned on. Then IC18 input 1B becomes LOW. IC18 1Y is fixed to LOW until the output voltage fails, and the convertor is stopped.



* Set OFF: VCC is supplied to 28V output, but it is turned off (transistor SW) in LVC (SC3611). So it is not supplied to the LCD driver.

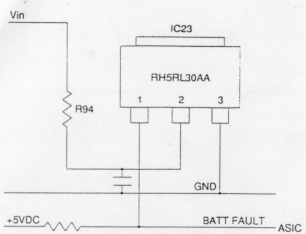


7. Power circuit (Boosting circuit)

LCD boosting circuit

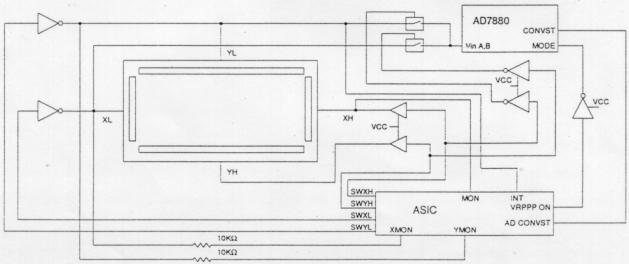
The power to operate the LCD is generated by the step-type chopper-system convertor as described below:
The 32.768MHz clock is inputted to the convertor 1A as the LCD DC CLK through the internal gate of ASIC. The LCD DC CLK is controlled by the ASIC gate and applied to the convertor when the power is turned on. When the power is turned off, it is fixed to LOW.
When the LCD DC CLK is supplied to the convertor and input 1B becomes HIGH, TR3 is turned ON/OFF from IC18 output 1Y. During ON period of TR3, coil L is charged with energy. During OFF period of TR3, coil L discharges the energy.

8. Low battery circuit



Voltage Vin inputted from the battery or the AC adapter is inputted to IC23 voltage detection input pin (2 pin). IC23 is monitoring.
When in low battery, if this voltage falls below 3V, IC23 judges it as BATT FAULT signal and turns 1 pin active.
BATT FAULT signal is inputted to ASIC. When ASIC detects this signal, it terminates the current operation forcibly and turns off the power.
The voltage falls to BATT FAULT voltage by battery exhaustion.
When the battery is replaced with new one and the power voltage recovers, the operation is started by turning on the power ON SW.
Low battery detection by the hardware is only BATT FAULT. Low battery display during the OS operation is performed by judging the battery voltage detected from the AD convertor with the software.
The 5V convertor output is monitored by IC21. When +5V DC output falls below 4.5V, the above BATT FAULT operation is performed. This is to protect the memory in case of abnormality such as break-down of the 5V convertor.

9. Tablet circuit



Tablet circuit description

* OS mode
The tablet control TR, the AD convertor, and the ASIC are used to detect the transparent tablet position.
The A/D convertor converts ????

converts the analog voltage into 12-bit data
tablet positions, ???? pressed ??? X, Y direction ???

(If the pressed level is judged as equal to or higher than the specified level, conversion is performed.)
The tablet applies a voltage in X and Y directions in time division with the control TR. In the X direction measurement, a voltage corresponding to the pressed position is outputted to YL. In the Y direction measurement, it is outputted to XL.
The ASIC controls the A/D convertor and the control TR.
To reduce power consumption in the OS mode, the tablet input interruption is detected with INIT signal by the ASIC. Only when there is a tablet input, the AD7880 is switched from the power save mode to the normal mode by the control of ASIC and the AD7880 is operated. (For switching from the power save mode to the normal mode, the AD7880 mode pin is used. When MODE = L, the power save mode. When MODE = H, the normal mode.)

* Diag mode
During a diag operation, INIT signal interruption is not used and the AD7880 always detects inputs of the X axis and the Y axis of the tablet.
Therefore, the tablet input operation differs between the OS operations and the diag operations. If the tablet operates normally only in the diag mode and does not operate normally in the OS mode, check MON, XMON, and YMON pins.

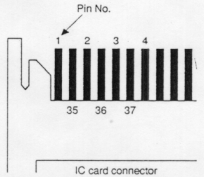
10. PCMIA card interface

The major function of the PCMIA card is to send and receive data between the card and the CPU or the system memory. Though ARM610 data bus is of 32 bits, the PCMIA data bus is of 16 bits. So 16-bit data are converted into 32-bit inside the ASIC and an access is made.
The PCMIA supports two types; the memory card type and the I/O card type.
For the corresponding memory card, PCMAIA 2.0 version mask ROM, EPROM, flash memory, and SRAM card can be used. (some cards may require installation of a special card driver.) the I/O card allows the use of a Modem and LAN.

Pin arrange-ment	Pin No.	PCMCIA	PCMCIA function. ( ) shows the function when the I/O card is operating.
1	1	GND	
2	35	GND	
3	2	D3	
4	36	–CD1	Card detection
5	3	D4	
6	37	D11	
7	4	D5	
8	38	D12	
9	5	D6	
10	39	D13	
11	6	D7	
12	40	D14	
13	7	–CE1	Card enable
14	41	D15	
15	8	A10	
16	42	–CE2	Card enable
17	9	–OE	Output enable
18	43	RFSH	Refresh
19	10	A11	
20	44	(–I/ORD)	Reservation (I/O READ)
21	11	A9	
22	45	(–I/OWR)	Reservation (I/O WRITE)
23	12	A8	
24	46	A17	
25	13	A13	
26	47	A18	
27	14	A14	
28	48	A19	
29	15	–WE/–PGM	Write enable
30	49	A20	
31	16	+RDY/–BSY	Ready/busy (–IREQ interruption request)
32	50	A21	
33	17	VCC	5V
34	51	VCC	5V
35	18	VPP1	Program power (Power for peripheral devices)
36	52	VPP2	Program power (Power for peripheral devices)
37	19	A16	
38	53	A22	
39	20	A15	
40	54	A23	
41	21	A12	
42	55	A24	
43	22	A7	
44	56	A25	
45	23	A6	
46	57	RFU	Reserved
47	24	A5	
48	58	+RESET	
49	25	A4	
50	59	–WAIT	Wait

Pin arrange-ment	Pin No.	PCMCIA	PCMCIA function. ( ) shows the function when the I/O card is operating.
51	26	A3	
52	60	(–INPACK)	Reserved (Input response)
53	27	A2	
54	61	–REG	Attribute memory space select
55	28	A1	
56	62	BVD2	Battery voltage detection (–SPKR digital sound signal)
57	29	A0	
58	63	BVD1	Battery voltage detection (–STSCHG card state change)
59	30	D0	
60	64	D8	
61	31	D1	
62	65	D9	
63	32	D2	
64	66	D10	
65	33	+WP	Write protect (16 bit I/O port)
66	67	–CD2	Card detection
67	34	GND	
68	68	GND	

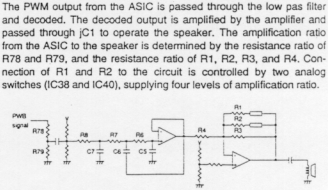
IC card connector



* Be careful that the pin arrangement of the IC card connector is irregular as shown above.

11. Sound control

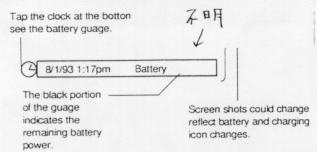
JUNIOR-1 sound output system is of 8 bit PWM using 10MHz as the basic clock. Sound PWM signal is generated inside the ASIC and outputted to IC4.
One of two operation amplifiers of IC4 is used as the low pass filter, and the other is used as the amplifier. The low pass filter characteristics are determined by R6, R7, R8, C5, C6, and C7.
The PWM output from the ASIC is passed through the low pas filter and decoded. The decoded output is amplified by the amplifier and passed through jC1 to operate the speaker. The amplification ratio from the ASIC to the speaker is determined by the resistance ratio of R78 and R79, and the resistance ratio of R1, R2, R3, and R4. Connection of R1 and R2 to the circuit is controlled by two analog switches (IC38 and IC40), supplying four levels of amplification ratio.

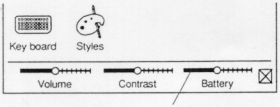


CHAPTER 3. NOTE FOR SERVICING

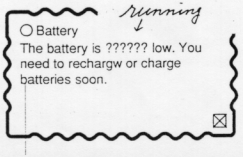
1. Monitoring the Main Batteries

Unless you plug Newton into an electrical outlet, it draws power from the main batteries when you use it. Here's how to check how much battery power you have left:





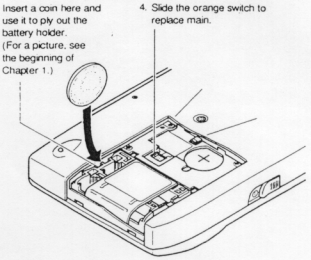
Open the extras drawer to look at the battery gauge.



Pay attention to the warnings that appear on the screen.

When you see this warning, you have about an hour of battery life left (depending on what you're doing). If you don't change the batteries in time, Newton will turn itself off.

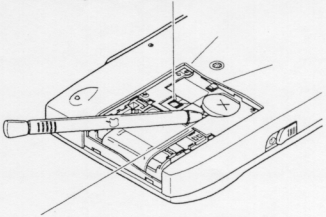
3. Use your thumb to slide off the panel that covers the batteries.



6. Remove the old AAA batteries and discard them in a legal and safe manner.
7. Insert four new AAA batteries, taking care to install them so they match the +/– polarity marked on the plastic holder. (If you're installing a Newton rechargeable battery pack, don't use the plastic and metal AAA battery holder.)
8. Put the battery holder back into Newton with the metal door face up and the coin slot to the left.
9. Slide the orange switch back to IN USE.
10. Replace the panel that covers the batteries.

- Replace the battery only with a lithium battery or its equivalent, as recommended by an authorized Apple dealer.
- Discard used batteries according to manufacturer's instructions.

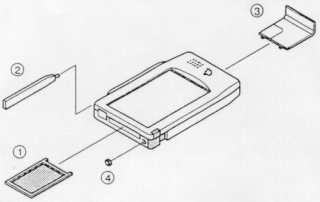
1. Turn off the Newton device.
2. Place Newton screen-side down onto a surface that won't damage the screen.
3. Use your thumb to slide off the panel that covers the batteries.
4. Slide the orange switch to replace backup.



5. Use the Newton pen (orsimilar object) to remove the old battery
6. Put in the new lithium battery # or its equivalent. Make sure the battery is + side up.
7. Slide the orange switch back to IN USE.
8. Replace the panel that covers the batteries.

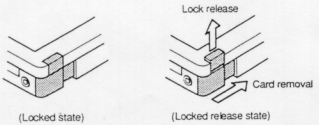
CHAPTER 4. DISASSEMBLY AND ASSEMBLY

1. Remove dummy card unit ①, pen unit ②, and battery cover unit ③ from the main body. Remove screw blind sheet ④.



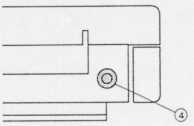
(1) Dummy card unit removal

Open and close the lock of the eject unit as shown below:

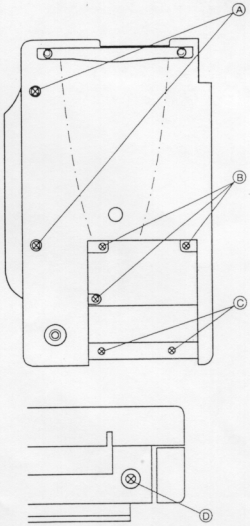


(Locked state) (Locked release state)

(2) Remove the screw blind sheet at the side of the card insertion hole.



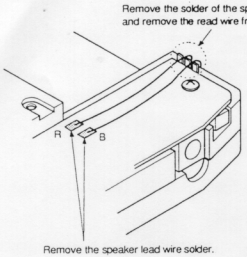
2. Remove the screws from the lower cabinet.
(Ⓐ 2 pcs., Ⓑ 3 pcs., Ⓒ 2 pcs., Ⓓ 1 pc.: Total 8 pcs.)



Remove the IR filter A. (Between chassis A and the lower cabinet.)

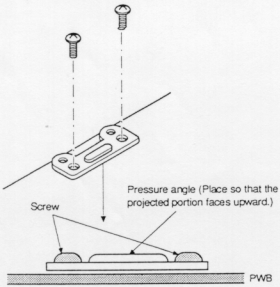
<Note> When attaching the screws, attach in the sequence of Ⓑ, Ⓒ, Ⓐ, and Ⓓ.

3. Speaker lead wire removal

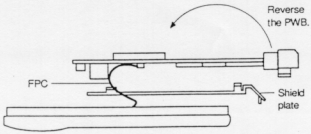


<Note> When soldering the lead wire of the speaker, solder at temperature of Max. 608 F for Max. 5 sec and do not mistake the lead wire color.

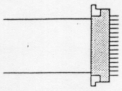
4. Pressure angle removal



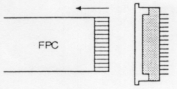
5. PWB unit removal



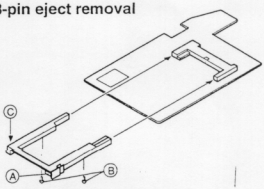
PWB FPC removal



<Note> When unlock the 40-pin connector, be careful not to damage it.



6. 68-pin eject removal

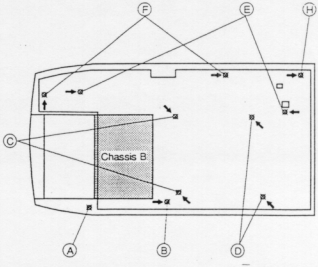


Remove two fixing screws Ⓑ of the eject unit.
Remove pawl Ⓐ from the PWB and pull out the unit.

<Note> when attaching the eject unit, lift section Ⓒ slightly and insert and attach it.

7. Chassis A removal

Remove one screw Ⓐ, one screw Ⓑ, two screws Ⓒ, two screw Ⓓ, two screws Ⓔ, and two screw Ⓕ.

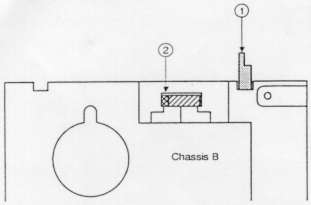


Do not remove screw Ⓗ.

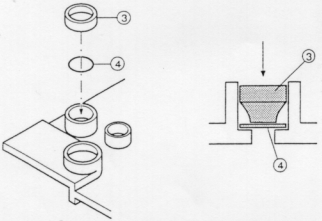
<Note> When attaching chassis A, tighten the screws in the sequence of Ⓐ to Ⓔ.

8. Note for assembly

(1) Chassis B unit check

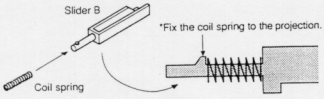


Insert the reset spacer/reset rubber.

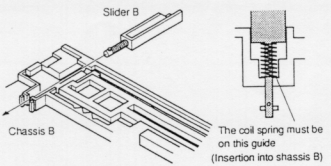


- While pushing slier B ①, slide battery replacement SW ② to the left edge and fix it temporarily.
- Check that reset rubber ③ and reset spacer ④ are inserted as shown in the figure. (No need to consider the rear and the surface of the reset spacer.)

(2) Coil spring attachment

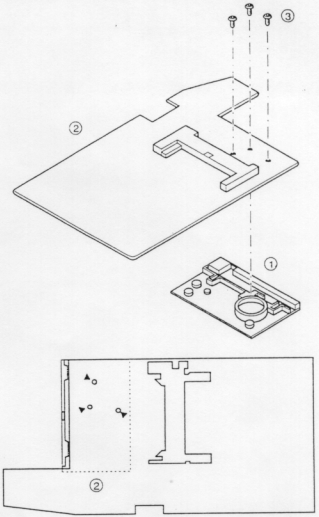


Slider B attachment



(3) PWB and chassis B unit attachment

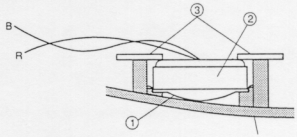
Fix chassis B unit ① to PWB unit ② with three screws ③.
(Set the screws at positions marked with ▲.)



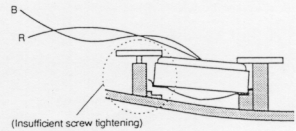
(4) Speaker attachment and lead wire treatment

- Insert speaker mesh ① into the center of the speaker hole before attaching speaker ②.
- When attaching the speaker, slightly press the center to install horizontally and fix it with two screws ③.

(GOOD)

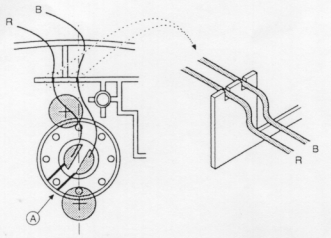


(NO GOOD)



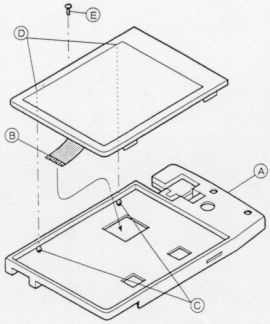
<Note>

- Do not allow contact between the lead wire of the speaker body and the screw. (Do not put the lead wire beneath the screw head as shown in Ⓐ.)
- Insert the speaker wire (B, R) into the groove in the upper cabinet.



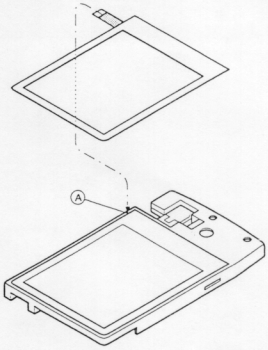
(5) LCD unit attachment

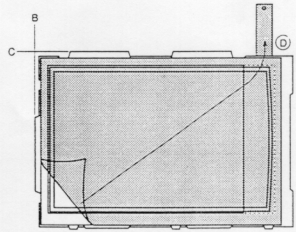
- Insert FPC terminal Ⓑ into chassis A Ⓐ, insert concave section Ⓓ of the LCD holder into the projected section Ⓒ in chassis A, and fix with screw Ⓔ.



(6) Tablet unit attachment

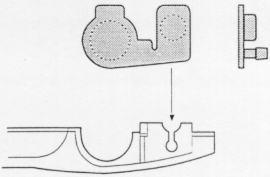
- Pass the tablet unit pressure section through chassis A and attach section Ⓐ.
- Fit the tablet mask external shape (upper side) with chassis A external shape. (B, C)





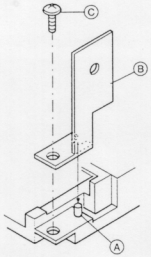
<Note> Attach the tablet protection sheet in the arrow direction and do not apply a pressure on pressure section Ⓓ.

(7) Connector cover attachment



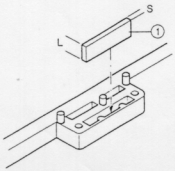
(8) Cabinet fixing angle attachment and screw tightening

- Attach the U-shaped section of cabinet fixing angle Ⓑ to positioning pin Ⓐ of chassis A and fix with screw Ⓒ.

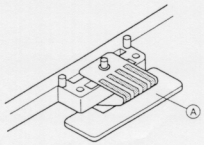


(9) Attach the cushion for touch pad, and fix the tablet pressure section.

- When inserting cushion for touch pad ① into chassis A, check L and S do not mistake them.



- Fix the tablet terminal as shown in Ⓐ.

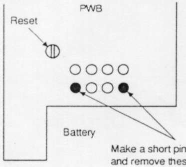


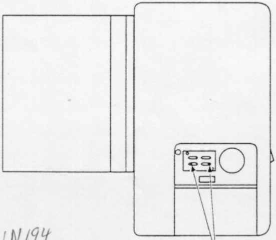
CHAPTER 5. DIAGNOSTIC

Tools necessary for diagnostic check of error position

1. Diag starter (Short pin, tweezers, etc.)
2. Loopback cable for serial check
3. 512KB SRAM card of the PCMCIA standard (Sharp CE301R is recommendable.)
4. A straight ruler of about 20 cm long

Diag starter using method
(When the back cabinet is removed:)





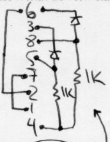
Short these two pads.
(There are eight pads in total. Do not mistake.)

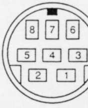
IN194
IN4148

Loopback wiring for serial check

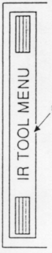
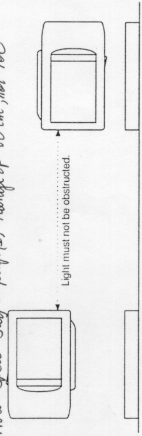
Pin No.	Signal
6	TXD+
3	TXD-
8	RXD+
5	RXD-
7	GPI
2	HSKI
1	HSKO

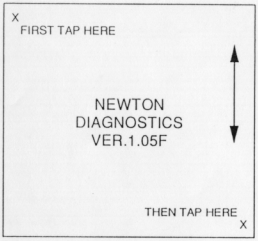
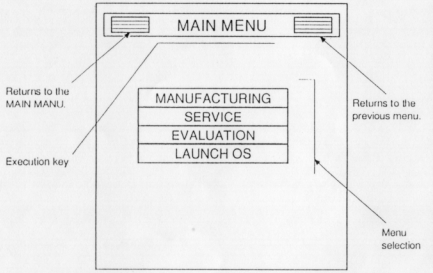
t always blue, orange, grey, green, purple, red, brown, yellow 4

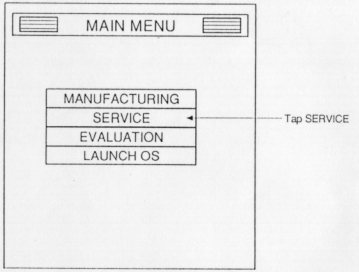
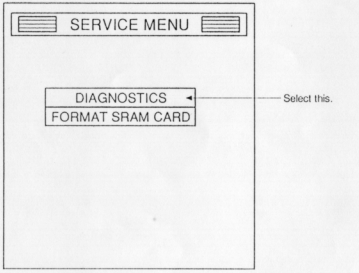


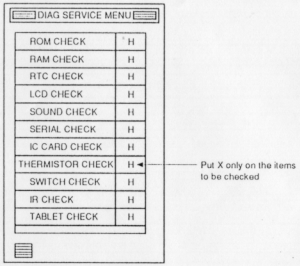


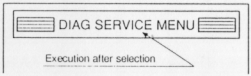
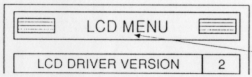
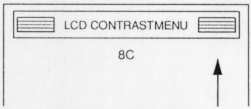
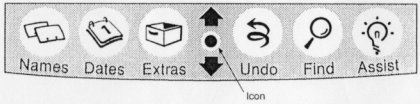
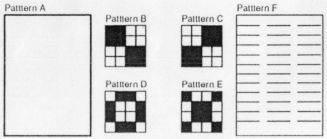
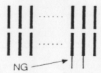
8pin serial port connectors

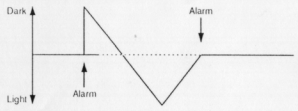
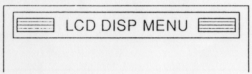
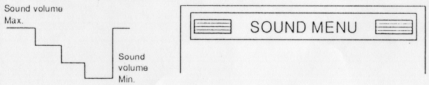
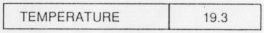
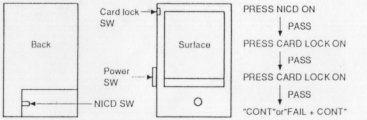
Item	Operating procedure	Display	Check item
		IR checker setting	
1	Set up the checker before checking.	* Checker setting procedure 1. Start the diag and press MANUFACTURING on the MAIN MENU. 2. Press CHECKING TOOL on the MANUFACTURING MENU. 3. Press IR CHECK TOOL on the CHECKING TOOL MENU. 4. As the STATUS displayed on the set is IDLE, press IR TOOL MENU to change to RUNNING.	
2	Put the checker and the machine to be checked face to face of the IR transmission/reception port on a white paper. (The paper should be placed on a horizontal surface.) Allow a distance of 1 m between the checker and the machine to be checked. To terminate the checker operation after setting, turn off the power.	Note: Specs say on page (1) range of 80 cm, not 100 	* IR check is automatically started immediately after completion of the previous check.

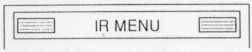
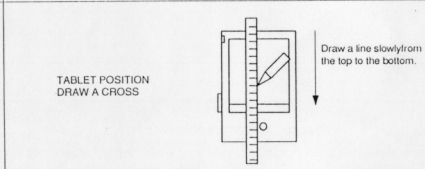
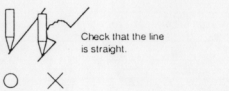
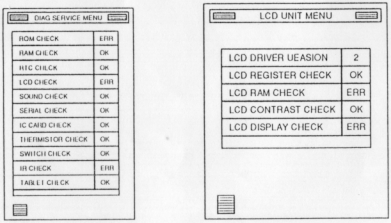
Item	Operating procedure	Display	Check item
1	Connect the Ac adapter. Set the diag starter. Press RESET, and remove the diag starter. Check that the display shown at right is given.		X Hold the Newton pen on the center of the X until it darkens and then lift the pen. Note: If the display is as shown in the left, the diagis not steated. In that case, repeat the procedure from the beginning.
2	On the screen of item 1, tap X of FIRST TAP HERE at the left upper corner, then tap X of THEN TAP HERE, and tap GO at the left bottom corner of the screen. Check that the display shown at right is given. Follow the procedures in the figure at right.		Note: If the display shown at left is not given, repeat the procedure from item 1.

Item	Operating procedure	Display	Check item
3	Select SERVICE on the MAIN MENU.		
4	Tap DIAGNOSTIC. When formatting the SRAM of PCMCIA.		

Item	Operating procedure	Display	Check item
5	Put X only on the items to be checked in the next menu. Since X is put on every item at the beginning, clear X of items which are not cleared by tapping X again.		✱ Before checking IR, set the IR checker in advance. ✱ Before checking the IC card, set th SRAM. ✱ Before checking the serial port, set the loopback cable in advance.

Item	Operating procedure	Display	Check item
6	Press DIAG SERVICE MENU, and ROM CHECK and ram CHECK are automatically executed.		✳ When performing the IR check, set the IR checker in advance. ✳ When performing the IC card check, set the SRAM in advance.
7	The operation is halted at LCD MENU. Then check the displayed VERSION of LCD DRIVER.		Check that the driver is of Version 2. Note: Do not tap CONT.
8	Press LCD MENU, and VRAM register check goes on to reach the LCD CONTRACT MENU.		Move up and down according to the displayed arrow and check that contrast is changed smoothly. After checking, adjust so that th display hexadecimal number of 2 digits becomes 8B or 8C.
9	Move up and down according to the displayed arrow to change contrast and fit the figure to 8B or 8C. Then tap the icon. In the case of OK, tap CONT, in the case of Not OK, tap FAIL.		
10	The external frame is displayed, and pattern B ~ F are alternatively displayed one by one every time when the Icon is tapped.		✳ Check that the external frame is completely displayed. ✳ Check that pattern B ~ F are free from defective display, blur, etc. ✳ Check that pattern F is free from blots under the lines. 

Item	Operating procedure	Display	Check item
11	Tap the icon, and contrast will change on pattern B and the alarm will sound.		✱ There is 4-sec interval between the first and the second alarm sounds. Check that the display contrast is changed smoothly as shown in the left figure. Check that the alarm sounds at the timing shown in the left figure.
12	If pattern A - F and automatic variation of contrast are proper, select CONT. If there is any defective point, select FAIL then CONT.		PASS | FAIL | CONT ✱ When FAIL is erroneously selected, select PASS again.
13	The sound menu is automatically started and the sound volume is changed in 4 steps. (It takes about 3 sec to terminate the process.)		Check that the sound volume is changed as shown in the left figure. (This menu is automatically operated and terminated.)
14	The THERMISTOR MENU is displayed and the temperature is displayed on the TEMPERATURE column. If it is OK, select CONT. In case of an error, select FAIL then CONT.		Check that the difference between the displayed temperature and the atmospheric temperature is within ±5 C.
15	According to the indication of "PRESS NICD ON" on the SWITCH MENU, press the switch. Check and press CONT.		Check that the display changes from OFF to ON when SW its pressed. (When the SW is released, the display changes from ON to OFF.) Note that the IC check is automatically performed after that.

Item	Operating procedure	Display	Check item
16	After completion of the SW MENU operation, the IR MENU is automatically performed and terminated. (It takes about 2 sec to terminate.)		For setting the checker unit, refer to the attached sheet. Setup and setting should be performed in advance to execution of the check.
17	Tap the tablets on the TABLET MENU in the sequence shown in the left column.	1. Tap heavily the center of INTERRUPT PRESS HERE. 2. Tap lightly the center of X PRESS HERE LIGHT. 3. Tap heavily the center of X PRESS HERE HEVY. 4. Tap lightly the center of Y PRESS LIGHT. 5. Tap heavily the center of Y PRESS HERE HEVY.	Center: Center of LCD.
18	The display is given as shown in the right. Put a scale and draw a line slowly from the top to the bottom.		
19	When the DIAG SERVICE MENU is completed, the PRODUCTION MENU shown in the right is given. Note that the LCD menu has the sub menu. When, therefore, the LCD menu is ERR, be sure to press LCD CHECK to check the sub menu.		"ERR" is displayed in the item which has an error. Check that.

CHAPTER 6. TROUBLESHOOTING

⁎ Troubleshooting (When a overcurrent flows:)

1. When the ON current is abnormally large:

If an excessively large ON current flows when the diag is started normally (the OFF current is normal), the booster system power element may be defective or a short-circuit may be in the wiring.
If both the ON current and the OFF current are abnormal, the 5V system power related element may be defective or a short-circuit may be in the wiring.
The +5V system current can be measured with the total of the currents flowing through R28 and R64.

2. When the OFF current is abnormally large:

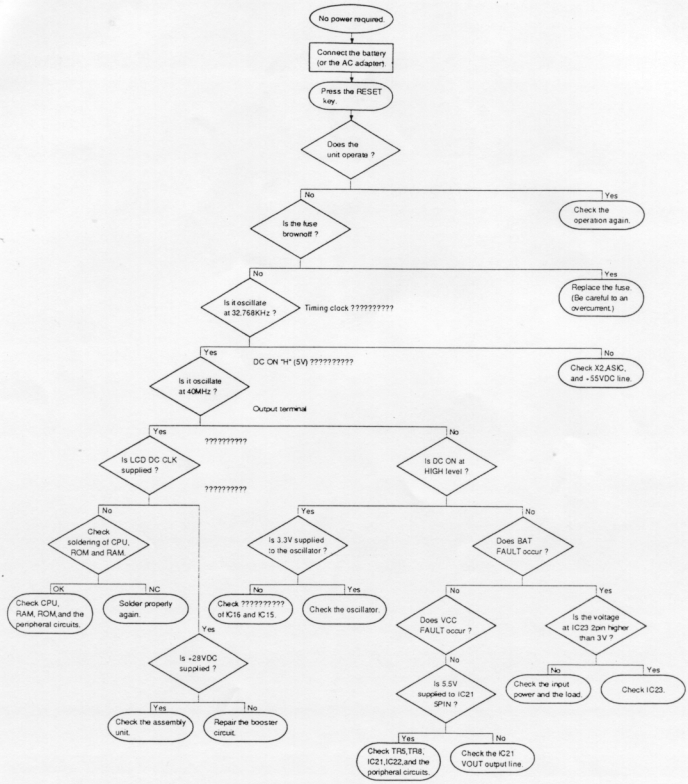
Under the OFF state, the power supply terminal may be defective, or a short-circuit may be in the +5V system power wiring. Or the power line is alive even the power switch is turned off.
(Especially be careful to the power system controlled by the DC ON.)
Under the OFF state, all the power supplies except for the +5V DC are normally cut off. So check the power source which is on.

3. When the backup current is abnormally large:

A large OFF current may cause a large backup current. Therefore, first check for the cause of the large OFF current.
When measuring the OFF current, a current is supplied from the main battery, and the backup current is supplied from the backup battery. The circuit operations are the same as the case of the OFF current measurement.

Note: This circuit operation is based on the third trial model.

✳ Troubleshooting
(The system doesn't start.)



VCC FAULT: When the VOUT is 4.5V or less, "L" is outputted from 3 pin (VDOUT) of the IC21. To prevent the IC21 3 pin from outputting "L" forcibly, float the IC21 3 pin.

BAT FAULT: When the battery voltage falls below 3V, "L" is outputted.

Note: This circuit operation is based on the third trial model.

✳ Circuit sequence

✳1: Power ON

1. When the power is supplied, if the input voltage is 3V or more, the power voltage is supplied to the IC21 (R55RMSH45B) 6 PIN (VDD) to output the regulate voltage of 5V.
   This VOUT voltage is supplied to each element as +5VDC.
   (Power system diagram)
2. When +5VDC is supplied, the power is supplied to the ASIC, starting oscillation of X2. The ASIC then turns DC ON signal active (from LOW to HIGH). When, however, the VCCD FAULT signal or the BAT FAULT signal is inputted to the ASIC, the DC ON signal turns non-active (from HIGH to LOW). If LOW signal is not inputted to the VCC FAULT and the BAT FAULT, the DC ON remains HIGH and is inputted to the IC16 (UMC4), turning the IC15 input (2 pin) HIGH, supplying 3.3V from the IC15 3 pin to the 40MHz oscillator (X1), starting oscillation of X1.
3. When the address buses of the CPU (ARM610), the ASIC, the SRAM, and the ROM operate normally, and when all data buses operate normally, and when the ROM data are rad normally, the ASIC outputs the LCD DC CLK from 36 pin. This LCD DC CLK signal serves as the reference oscillation clock for each booster circuit.
   After that, the ASIC turns 31 pin LCDLVCON to HIGH, activating the LVC (SC3611), and displaying the LCD screen.
   The system is started in the above sequence.

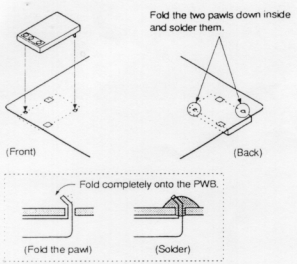
✳2: When the power is turned off by the software:

1. When the power is turned off by the power switch operation on the OS, or when it is turned off during a diag operation, the ASIC performs OFF process of each gate, turns the DC ON to LOW, and stops 40MHz clock. After that, the RAM, the ASIC, etc. are backed up by +5VDC.
2. This state is held until the command of power ON is given to the ASIC by POWER SW operation or software control. However, when the power voltage falls below 3V, the IC23 inputs the LOW level of BAT FAULT signal to the ASIC. In this case, the system is not restarted until the input voltage rises to 3V or more. In addition, the memory data are not retained if the backup voltage is supplied. The current which is supplied from the input power to the unit is the OFF current of the unit.

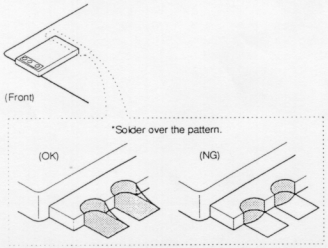
✳3: When the backup battery is set, the power is turned off by the software, and the input power voltage is cut off:
The circuit operates similarly to the descriptions in ✳2. When the input power voltage is cut off, the backup battery supplies the power to +5VDC.
The current which is supplied from the backup battery to the unit is the backup current of the unit.

Note: This circuit operations are based on the third trial model.

(1) IR unit attachment and soldering

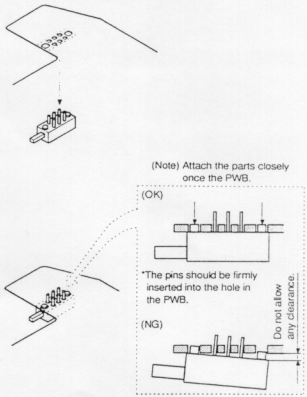


※ When folding the pawls, use the base plate in order not to apply a stress to the PWB.



※ Soldering temperature should be Max. 320°C (within 5 sec).

(2) Ni-Cd detection switch positioning and soldering

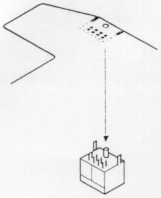


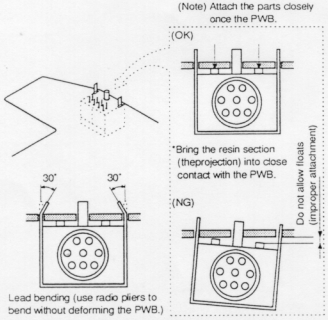
※ If there is a float (improper attachment), Ni-Cd detection cannot be performed in the set condition.

※ Use solder of 0.8 (diameter). (No need to cut.) (KR19RMA, diameter of 0.5)

※ Soldering temperature should be Max. 320°C (within 5 sec). (Excessive heat may cause malfunctions.)

(3) 8 pin jack positioning, lead bending and soldering



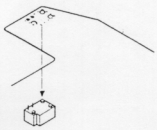


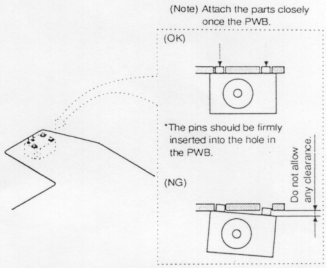
⁎ Soldering temperature should be Max. 320˚C (within 5 sec).

⁎ If there is a float, the 8 pin cable cannot be inserted under the set state.

⁎ Soldering is made in 11 positions.

(4) 2 pin jack positioning and soldering



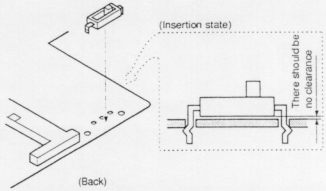


⁎ Soldering temperature should be Max. 320˚C (within 5 sec).

⁎ If there is a float, the 2 pin cable cannot be inserted under the set state.

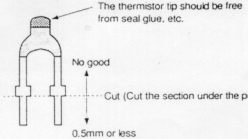
(5) Power ON/OFF switch positioning and soldering

⁎ If there is a float, the power ON/OFF control may be malfunction under the set state.



⁎ Soldering temperature should be Max. 320˚C (within 5 sec).

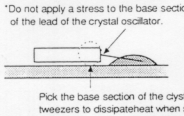
(6) Thermistor lead cutting and soldering temperature



* Soldering temperature should be Max. 300°C (within 5 sec).
(Use a soldering iron with temperature adjustment function.)

* Solder the thermistor lead so that it is covered completely.

(7) Soldering temperature of the crystal oscillator should be Max. 300°C (within 5 sec).



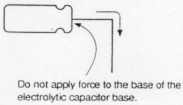
* Do not apply a stress to the base section of the lead of the crystal oscillator.

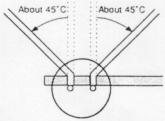
* Soldering temperature should be Max. 300°C (within 5 sec).
(Use a soldering iron with temperature adjustment function.)

* Note: Be careful to keep the soldering iron away from the ????????? of the crystal oscillator.

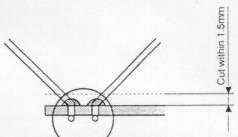
↑ ?

(8) Electrolytic capacitor forming and lead cutting





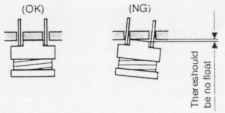
*Bend the electrolytic capacitor lead, temporarily fix it , and solder it.



* When cutting the electrolytic capacitor lead, be careful not to damage the other adjacent parts with nippers.

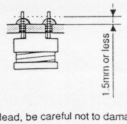
* Soldering temperature should be Max. 320°C (within 5 sec).

(9) Coil soldering and lead cutting



* Insert the projection closely into the PWB hole. (There should be no float.)

* If there is a float, the cabinet is damaged.



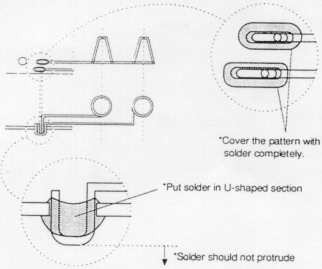
* When cutting the lead, be careful not to damage the adjacent chips and parts.

* Soldering temperature should be Max. 320°C (within 5 sec).

(10) Main power pins (+)(–) soldering (Soldering conditions)

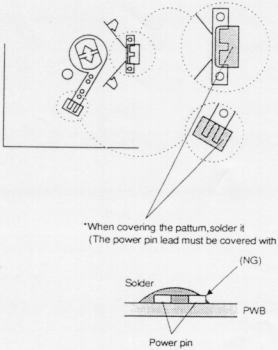
Conditions	(+)(–) pins
Soldering capacity	40W
Soldering tip temperature	320 ~ 360°C
Soldering time	4 ~ 5 sec.
Solder diameter 0.8	KR19RMAφ0.8

※ There should be no solder balls (especially on the pattern.)



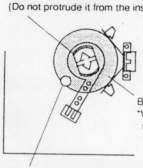
(11) Backup battery pins (+)(–) soldering (Soldering conditions)

Conditions	(+)(–) pins
Solder capacity	40W
Soldering tip temperature	320 ~ 360°C
Soldering time	4 ~ 5 sec.
Solder diameter 0.8	KR19RMAφ0.8



(12) Backup battery sheet attachment

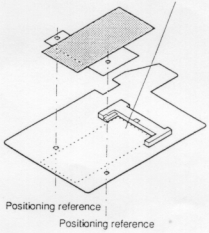
*Attach to the inside line of the backup battery terminal (-). (Do not protrude it from the inside line.)



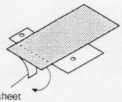
*Attach the sheet so that it does not cover the PWB hole (for slider C).

(13) IC card insulation sheet attachment

① Visually check the shaded section with a magnifier. (Must be free from solder ball and foreign materials.)

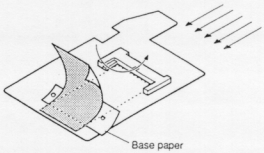


② Remove the separation sheet from one side.



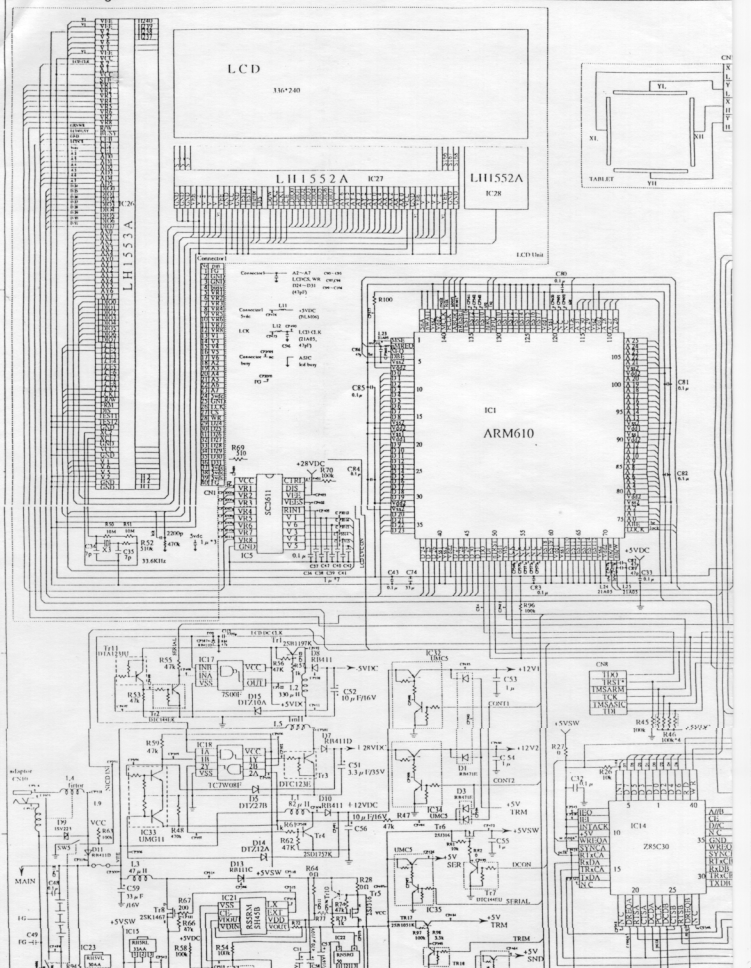
② Remove the separation sheet in the other side and attach the insulation sheet.

*When removing the separation sheet, operate the diswcharge blower.



※ When attaching, press with fingers to attach firmly. (Use special care to attach the fringes without floats or bubbles.)

1. Circuit Diagram



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				1993.05.24