PCMCIA 2.1 Compliant FLASH Memory Cards - 2 to 20 Megabyte Card Features Intel 28F008SA Series II Devices for 5 and 12 Volt Operations

Description

These Centennial products are high quality PCMCIA 2.1 compliant Type I FLASH memory cards which feature an array of 2 to 20 Intel® 28F008SA 8 Megabit FLASH components. Because of the reliable FLASH technology used, data retention is assured without the need for battery back-up of any kind, even when system power is removed.

These products offer memory capacities of between 2 to 20 Megabytes with a 64 Kbyte block erase resolution. Memory blocks that are not busy with erase operations, may be accessed by both read and write commands without concern for on going operations in other blocks. Additionally data may be handled in either 8 bit or 16 bit bus modes.

These features, packaged in a quality PCMCIA housing by our ISO 9001 certified production team, make Centennial memory cards especially desirable for a wide variety of custom applications that utilize PC Card slots such as PDAs and other handheld devices.

Features

- PCMCIA 2.1 compliant
- FLASH Architecture, non volatile memory
- Standard 200 ns Access Time from Standby
- Byte-wide and Word-wide access
- Embedded Program/Erase Algorithms
- Erase Suspend/Resume Feature
- 64 Kilobyte Block Erase Resolution
- High Write Endurance
  100,000 Write/Erase Cycles Min.
- Dedicated Attribute Memory EEPROM
- Extremely Low Power Consumption
  - 150 uA Max. Standby Current (CMOS)
  - 75 mA Max. Byte Write Current
  - 50 mA Max. Block Erase Current
- ISO 9001 Quality Controls

PIN DESCRIPTION

Signal	Name	Function
A[25:0]	Address Bus	Address Inputs, A25-A0
D[15:0]	Data Bus	Data Input/Outputs
/OE	Output Enable	Active Low for Read
/WE	Write Enable	Active Low for Write
/CE1	Card Enable Low Byte	Active Low for Read/ Write Even Byte
/CE2	Card Enable High Byte	Active Low for Read/ Write Odd Byte
/REG	Register Select	Active Low enables Attribute Memory
WP	Write Protect	Output Signal indicates the WP switch state
/VS1, /VS2	Voltage Sense 1, 2	Voltage Sense Outputs
/CD1, /CD2	Card Detect Signals 1, 2	Tied to GND
Vpp1, Vpp2	Program Voltages 1, 2	Device program voltages +12 V ±5%
V_{CC}	Power Supply	Power Supply Voltage, +5.0V ±5%
GND (V_{SS})	Ground	Card Ground

PIN ASSIGNMENTS

Pin #	Signal	I/O	Function		Pin #	Signal	I/O	Function	
1	GND		Ground		35	GND		Ground	
2	D3	I/O	Data Bit 3	PL	36	/CD1	O	Card Detect - Grounded	
3	D4	I/O	Data Bit 4	PL	37	D11	I/O	Data Bit 11	PL
4	D5	I/O	Data Bit 5	PL	38	D12	I/O	Data Bit 12	PL
5	D6	I/O	Data Bit 6	PL	39	D13	I/O	Data Bit 13	PL
6	D7	I/O	Data Bit 7	PL	40	D14	I/O	Data Bit 14	PL
7	/CE1	I	Card Enable Low byte	PH	41	D15	I/O	Data Bit 15	PL
8	A10	I	Address Bit 10		42	/CE2	I	Card Enable High byte	PH
9	/OE	I	Output Enable	PH	43	/VS1		Vltg Sense Signal 1- Open	
10	A11	I	Address Bit 11		44	*RFU*		*Reserved For Future Use*	NC
11	A9	I	Address Bit 9		45	*RFU*		*Reserved For Future Use*	NC
12	A8	I	Address Bit 8		46	A17	I	Address Bit 17	
13	A13	I	Address Bit 13		47	A18	I	Address Bit 18	
14	A14	I	Address Bit 14		48	A19	I	Address Bit 19	
15	/WE	I	Write Enable	PH	49	A20	I	Address Bit 20	PL
16	/BUSY	O	Ready Busy Signal	NC	50	A21	I	Address Bit 21 **(Note 1)**	PL
17	V_{CC}		Power Supply		51	V_{CC}		Power Supply	
18	*Vpp1*		*Program Voltage 1*		52	*Vpp2*		*Program Voltage 2*	
19	A16	I	Address Bit 16		53	A22	I	Address Bit 22 **(Note 1)**	PL
20	A15	I	Address Bit 15		54	A23	I	Address Bit 23 **(Note 1)**	PL
21	A12	I	Address Bit 12		55	A24	I	Address Bit 24 **(Note 1)**	PL
22	A7	I	Address Bit 7		56	A25	I	Address Bit 25 **(Note 1)**	PL
23	A6	I	Address Bit 6		57	/VS2		Vltg Sense Signal 2- Open	
24	A5	I	Address Bit 5		58	RESET	I	Hardware RESET	NC
25	A4	I	Address Bit 4		59	WAIT	O	Wait State Control **(Note 2)**	NC
26	A3	I	Address Bit 3		60	*RFU*		*Reserved For Future Use*	NC
27	A2	I	Address Bit 2		61	/REG	I	Register Select	PH
28	A1	I	Address Bit 1		62	/BVD2	O	Batt. Voltage Detect 2	PH
29	A0	I	Address Bit 0	PL	63	/BVD1	O	Batt. Voltage Detect 1	PH
30	D0	I/O	Data Bit 0	PL	64	D8	I/O	Data Bit 8	PL
31	D1	I/O	Data Bit 1	PL	65	D9	I/O	Data Bit 9	PL
32	D2	I/O	Data Bit 2	PL	66	D10	I/O	Data Bit 10	PL
33	WP	O	Write Protect		67	/CD2	O	Card Detect - Grounded	
34	GND		Ground		68	GND		Ground	

Notes :

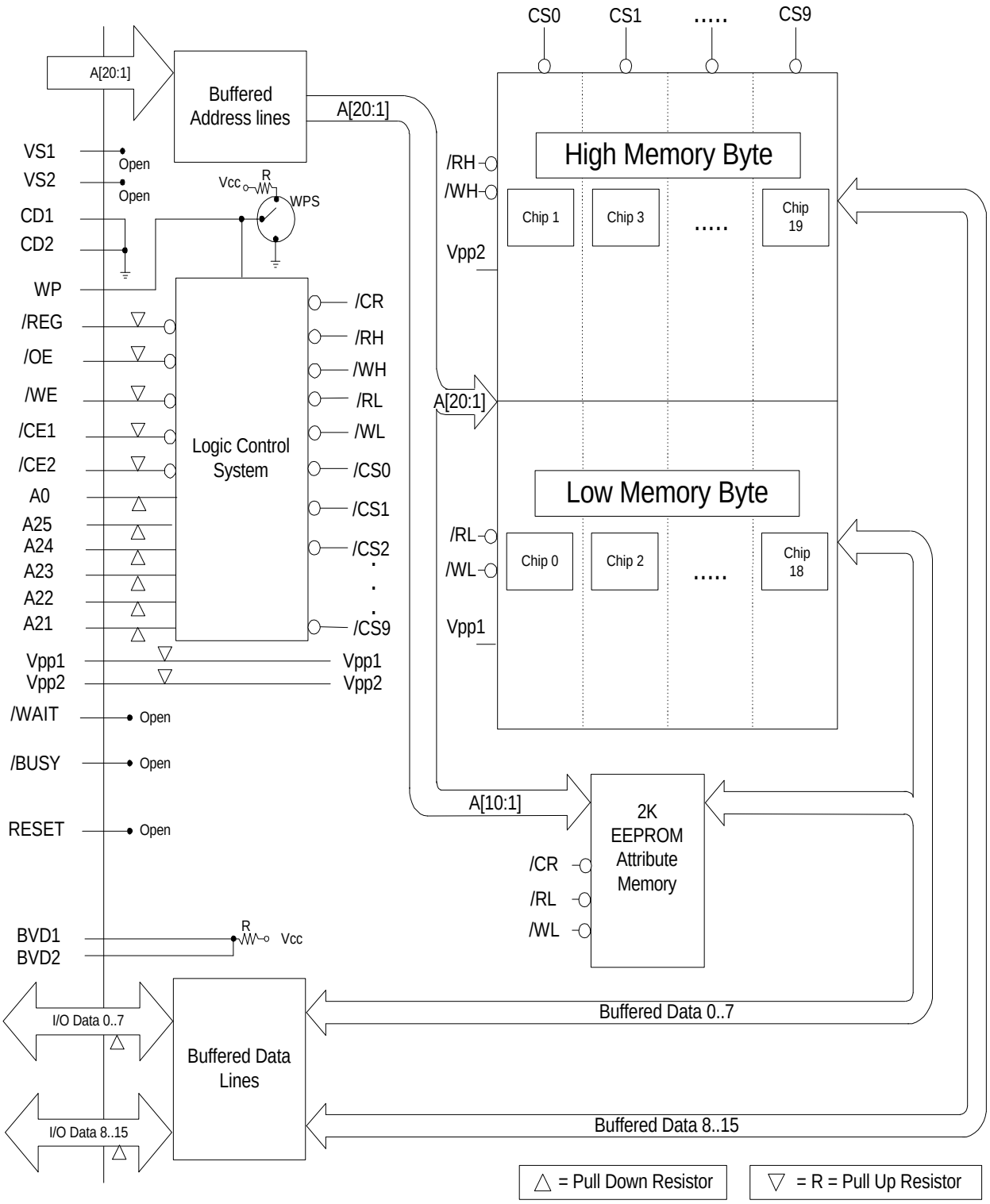
1. *The full 64Mbyte address space is decoded regardless of Card capacity.*
2. *There are no wait states generated by these cards. This signal must be pulled high by the Host socket.*

Legend :

I = *Input to card only*
O = *Output from card only*
I/O = *Bi-directional signal*
PH = *Pulled High (10 - 50K Typ.)*
PL = *Pulled Low (100K Min.)*
NC = *Not Connected*

Functions of the shaded pins are not used.

FUNCTIONAL BLOCK DIAGRAM



Minimum 100K Ω Typical 10K to 50K Ω

COMMON MEMORY BUS OPERATIONS

Operation	/REG	/CE2	/CE1	/OE	/WE	A0	D8-D15	D0-D7
READ								
Read Even (x8)	H	H	L	L	H	L	High -Z	**Data Out-Even**
Read Odd (x8) **(Note 1)**	H	H	L	L	H	H	High -Z	**Data Out-Odd**
Read Odd (x8)	H	L	H	L	H	X	**Data Out-Odd**	High-Z
Read Word (x16)	H	L	L	L	H	X	**Data Out-Odd**	**Data Out-Even**
WRITE/ERASE								
Write Even (x8)	H	H	L	H	L	L	High -Z	**Data In-Even**
Write Odd (x8) **(Note 1)**	H	H	L	H	L	H	High -Z	**Data In-Odd**
Write Odd (x8)	H	L	H	H	L	X	**Data In-Odd**	High-Z
Write Word (x16) **(Note 2)**	H	L	L	H	L	X	**Data In-Odd**	**Data In-Even**
INACTIVE								
Card Output Disable	X	X	X	H	X	X	High-Z	High-Z
Standby	X	H	H	X	X	X	High-Z	High-Z

Notes:

1. *Byte access - Odd. In this x8 mode, A0 = V_{IH} outputs or inputs the "odd" byte (high byte of the x16 word on D0 - D7). This is accomplished internal to the card by transposing D8-D15 to D0-D7.*
2. *During 16-bit write and erase operations one IC of a device pair may complete the operation prior to the other. It is therefore necessary to poll both components before considering the operation complete.*

Legend:

$H = V_{IH}$
$L = V_{IL}$
X = Don't Care

Warning: Raising address lines to voltages levels above CMOS levels is not permitted. Applying voltages above these levels will destroy the card. Any attempt to identify memory components in this way is not permitted.

ATTRIBUTE MEMORY BUS OPERATIONS

Pins/Operation	/REG	/CE2	/CE1	/OE	/WE	A0	D8-D15	D0-D7
READ (Note 1)								
Read Even (x8)	L	H	L	L	H	L	High -Z	**Data Out-Even**
Read Odd (x8) **(Note 2)**	L	H	L	L	H	H	High -Z	Data Out-Odd Not Valid
Read Odd (x8) **(Note 2)**	L	L	H	L	H	X	Data Out-Odd Not Valid	High-Z
Read Word (x16) **(Note 2)**	L	L	L	L	H	X	Data Out-Odd Not Valid	**Data Out-Even**
WRITE (Note 1)								
Write Even (x8)	L	H	L	H	L	L	High -Z	**Data In-Even**
Write Odd (x8) **(Note 3)**	L	H	L	H	L	H	High -Z	Data In-Odd Not Valid
Write Odd (x8) **(Note 3)**	L	L	H	H	L	X	Data In-Odd Not Valid	High-Z
Write Word (x16) **(Note 3)**	L	L	L	H	L	X	Data In-Odd Not Valid	**Data In-Even**
INACTIVE								
Card Output Disable	X	X	X	H	X	X	High-Z	High-Z
Standby	X	H	H	X	X	X	High-Z	High-Z

Note:

1. *Refer to the data sheets for the Microchip 28C16A EEPROM for details on programming the attribute memory.*
2. *Data Read operations will produce data information that has no valid meaning for the Odd byte of information.*
3. *Data Write operations may be initiated, however data information for the Odd byte will not be stored.*

Legend:

$H = V_{IH}$
$L = V_{IL}$
X = Don't Care

Warning: Raising address lines to voltages levels above CMOS levels is not permitted. Applying voltages above these levels will destroy the card. Any attempt to identify memory components in this way is not permitted.

PIN DESCRIPTIONS

Vcc
Card Power Supply

Power input required for device operation. The Vcc must be 5.0 V ± 5% (4.75V to 5.25V).

GND
Card Ground

The V_{ss} pins of all IC components and related circuitry are connected to this card ground, which must be connected to the Host system's ground.

NC
Not Connected

These pins are physically not connected to any circuitry.

A0-A25
Address Bus

These signals are address input lines that are used for accesses to card memory. A0 is used to select the odd or even bank of memory components. A21 through A25 select which Device Pair of ICs will be accessed. A1 through A20 are used to select the specific address that is to be accessed on an individual memory component.
"No Addr. Wrap" option has the full 64Mbyte address space decoded regardless of card capacity. "Addr. Wrap" option doesn't decode the upper address lines. This results in an address wrap around effect. For example, when accessing 4MB card, address 000000h is effectively repeated in 4MB intervals at addresses 400000h, 800000h, etc. Attempting to address any of these locations would access the same physical location as 000000h.

/OE
Output Enable Signal

This active low input signal output data information.

/WE
Write Enable Signal

This active low input signal controls memory write functions and is used to strobe data into the card memory.

WP
Write Protect Signal

This output signal indicates status of card write operations which have been disabled by the Write Protect Switch (WPS). When the signal is asserted high, card write operations are disabled. When this signal is asserted low, card write operation function normally.

/CE1, /CE2
Card Enable

These are active low inputs used to enable the card memory. /CE1 accesses the low bank of memory, which provides storage for even numbered bytes. /CE2 accesses the high bank of memory, which provides storage for odd numbered bytes. During byte-wide operations these Card Enable signals are used in conjunction with address line A0 to access even or odd bytes of data. The memory card is de-selected and power consumption is reduced to stand-by levels when both /CE1 and /CE2 are driven high.

D0-D15

/REG
Register Select Signal

This active low input signal enables access to the Attribute memory EEPROM. Attribute memory is typically used to store the CIS file, which contains specific card information. Access to common memory is not possible when /REG is asserted low.

RESET
RESET Signal

This is an active high input signal that normally is used by the Host to place the card in the deep power down mode of operation. On these cards this signal is Not Connected.

/WAIT
Extended Bus Cycle

This active low output signal delays completion of a memory access operation. There are no wait states generated by these memory cards. For this reason the /WAIT signal is left open. It is the responsibility of the Host to pull this signal high to prevent false activation.

/BUSY
Ready Busy Signal

This active low output signal normally indicates that at least one memory device in the card is busy performing a task. On these cards this signal is Not Connected.

/CD1, /CD2
Card Detect

These pins are tied directly to ground and are used by the Host system to detect the presence of the card. If /CD1 and /CD2 are not both detected low by the Host, then the card is not properly inserted.

/VS1, /VS2
Voltage Sense Signals

The Voltage Sense Signals notify the socket of the card's Vcc requirements on initial power up. When both /VS1 and /VS2 are open, as is the case on these cards, the card is identified to the Host system as a 5V only card.

/Vpp1, /Vpp2
Program and Peripheral Voltages

These signals are used to supply additional programming voltages for memory devices that require programming voltages other than the Vcc supply. These memory cards require Vpp voltages of +12V ±5%.

/BVD1, /BVD2
Battery Voltage Detect

These pins are normally used to indicate the status of an internal card battery. Since FLASH cards do not require or use a battery, these signals are internally pulled high by a resistor.

MANUFACTURER'S IDENTIFICATION CODE TABLE

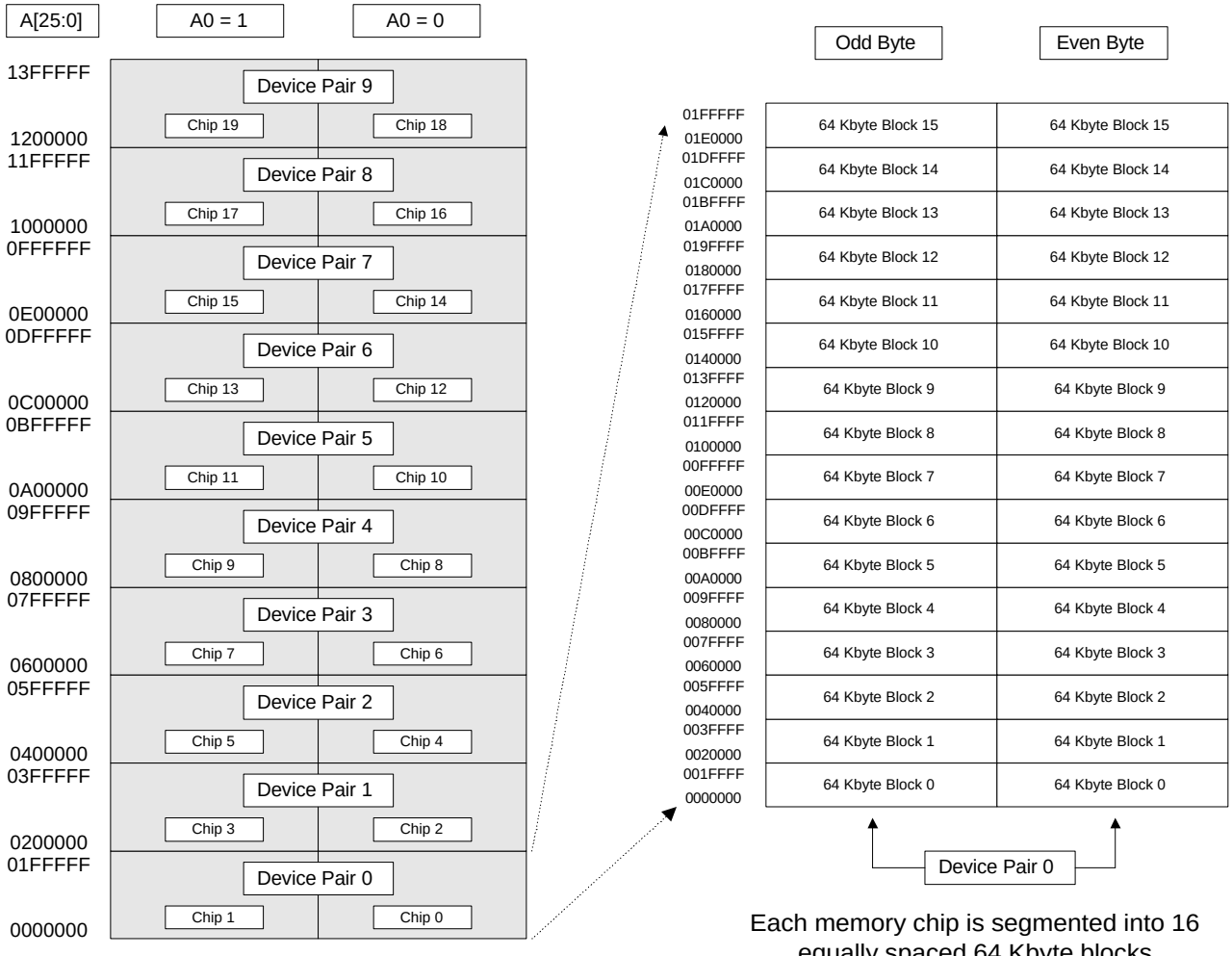
Device	Manufacturer	Hex Data		Operational Voltages	
		Manufacturer Code	Device Code	V_{CC}	V_{PP}
28F008SA	Intel	89h	A2h	5V ± 5%	12V ±5%

The component manufacturer and device ID codes of each common memory component may be read from the Card Information Structure (CIS), or directly from each memory device. The CIS file is located in the Attribute Section of the card memory. Typically the CIS is stored in the EEPROM.

Directly reading the IDs from a memory component may be done by initiating the embedded Read Identifier Codes Command (See Command Definitions Table for command sequence and codes). Once the appropriate command sequence codes have been written to a device, a read operation at chip address 00000h will return the Manufacture ID code and a read at 00001h will return the device ID code for the specific component use on the Card. This mode may be exited by initiating another valid command operation.

For complete details of these memory devices refer to the manufacturers published data sheets.

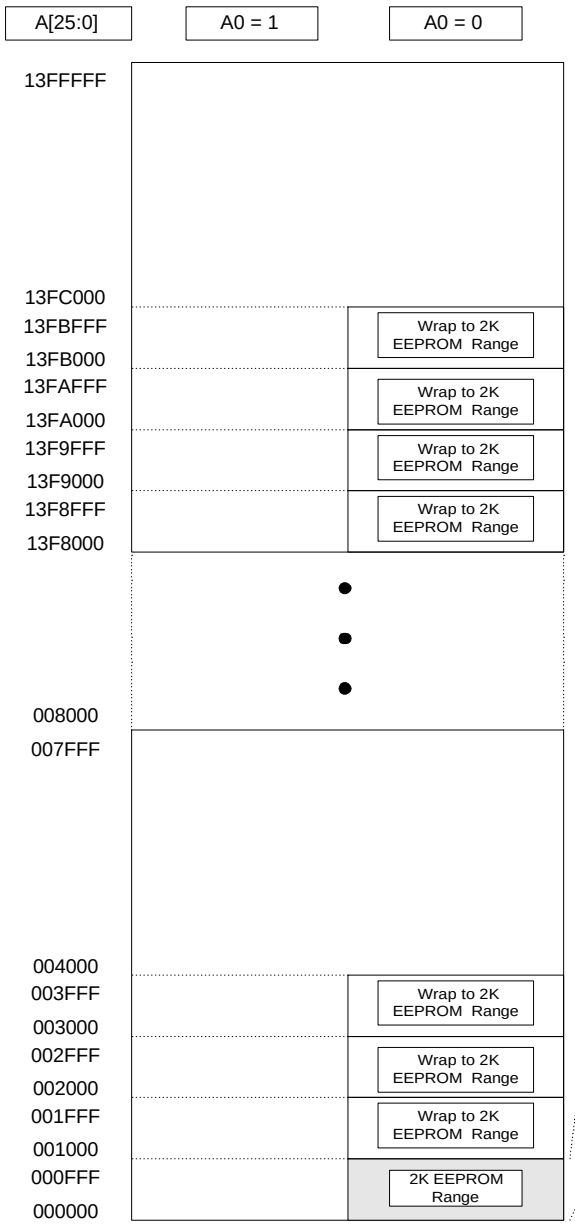
CARD COMMON MEMORY MAP



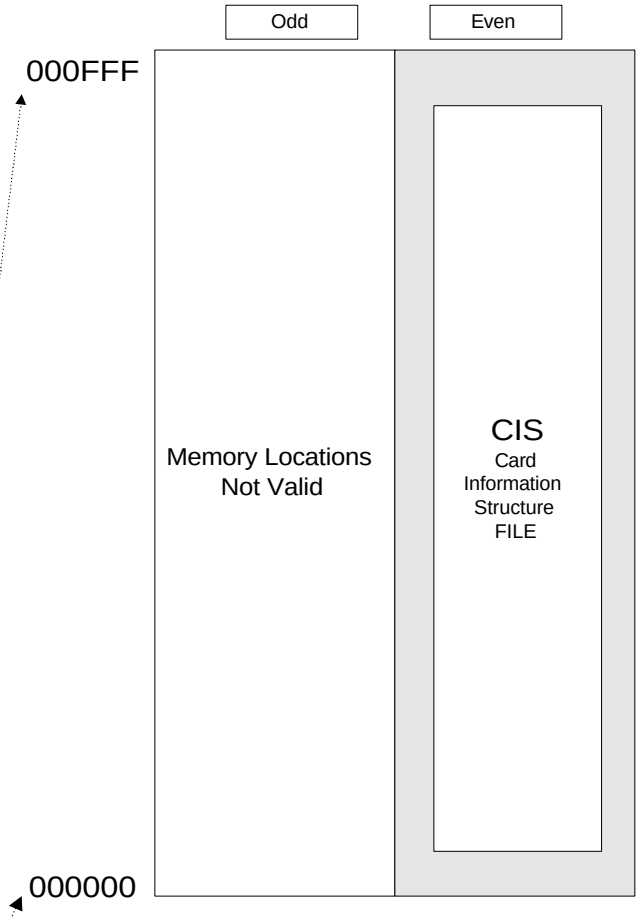
Each Device Pair represents 2 MBytes of Card memory.

Each memory chip is segmented into 16 equally spaced 64 Kbyte blocks

ATTRIBUTE MEMORY MAP



The CIS file is located only in even bytes of the card memory.



Attribute Memory Wrap around addressing occurs at every 2K increments.
The EEPROM is deactivated, whenever A14 = 1.

Addresses above 008000h wrap around to the same location as 000000h at every 32K intervals.

COMMAND DEFINITIONS TABLE

The Command definitions listed in the table below are for Common Memory devices only.

Command Code Sequence	Bus Cyc.	1st Bus Cycle				2nd Bus Cycle			
		Bus Opr	Addr	Data		Bus Opr	Addr	Data	
				Even	Odd			Even	Odd
Read Array	1	WRT	X	FFh	FFh				
Read Identifier Codes	≥2	WRT	X	90h	90h	RD	IA	ID	ID
Read Status Register	2	WRT	X	70h	70h	RD	X	SRD	SRD
Clear Status Register	1	WRT	X	50h	50h				
Block Erase	2	WRT	BA	20h	20h	WRT	BA	D0h	D0h
Byte Write	2	WRT	WA	40h	40h	WRT	WA	WD	WD
Alternate Byte Write	2	WRT	WA	10h	10h	WRT	WA	WD	WD
Erase Suspend / Resume	1	WRT	X	B0h	B0h				

Data is latched on the rising edge of /WE (See CARD TIMING CHARACTERISTICS).

Only those commands listed in the above table should be used. Commands not shown in the above table are reserved by the manufacturer for future device implementation.

Legend:

RD = Read operation
WRT = Write operation

X = Any valid address with in a memory device
IA = Identifier Code Address
BA = Address to the block being erased
WA = Address of the memory location to be written

SRD = Data read from status register
WD = Data to be written at location WA
ID = Read identifier code data

Read Array Command :

Cards may be read in Byte wide or Word wide modes. In Word-Wide mode, each byte of memory is independently read from each device pair. Each memory device in the card may read at different rates. Therefore the Host should wait until each byte has a valid data output (See MEMORY BUS OPERATIONS Table for specific Control line States and CARD TIMING CHARACTERISTICS for timing information).

On power up of the Card, each memory chip automatically defaults to Read Array state in order to prevent spurious data changes during power up, and does not require an additional Read command in order to begin reading data from memory at this time. This operation mode can also be initiated by writing the command code to the internal Write State Machine (WSM) of an individual memory device (See Command Definitions Table). The device remains enabled for read operations until another command is written to the WSM of that device.

Read operations may also be performed after a Block Erase Suspend or Byte Write Suspend command has been initiated (See Sector Erase Suspend Command and Byte Write Suspend Command).

Read Identifier Codes Command :

The identifier code operation is initiated by writing the Read Identifier Codes Command (See Command Definitions Table) to the Write State Machine (WSM) of an individual memory device. Following the command, a read from the chip addresses shown in the table below recalls specific information regarding the chip manufacture and device code.

To terminate the Read identifier Code operation, another valid command must be written to the CUI.

Chip Address A[21:1]	Information / Bit Status	Data
00000h	Manufacture Code	89h
00001h	Device Code	A6h

Standby Mode of Operation :

During any card operation only certain memory devices are active. Those that are not involved in a specific operation and are not directly made active by control signals can be placed into a reduced power mode by setting the /CE1 and /CE2 signals to a high logic state. Data output bits are then placed in a high-impedance state, independent of /OE. If a device is deselected during block erase or byte write operations, the device continues functioning normally until the operation is completed. At which point the device then enters the Standby Mode.

Each chip may be brought out of standby mode and made active by setting the chip enable signals to a low logic value (See MEMORY BUS OPERATIONS Table for specific control line states, see also DC CHARACTERISTICS for the standby current value).

Block Erase Command :

Block Erase is executed one block at a time and initiated by a two cycle command written to the WSM of a memory device (See Command Definitions Table). The erase operation command requires any valid address within a block and will change all data within that block to FFh. The WSM of each memory device will handle all block preconditioning, erase, and verify operations and also automatically updates the device status register data. The Host can detect completion of the operation by analyzing the status register SR7 data bit of the device. However, in order to determine if an operation has completed successfully without encountering any errors, the status register bits SR5, SR4, and SR3 of the memory device should also be checked (See Status Register Definitions Table).

A system designer has the following choices when initiating the Block Erase Command:

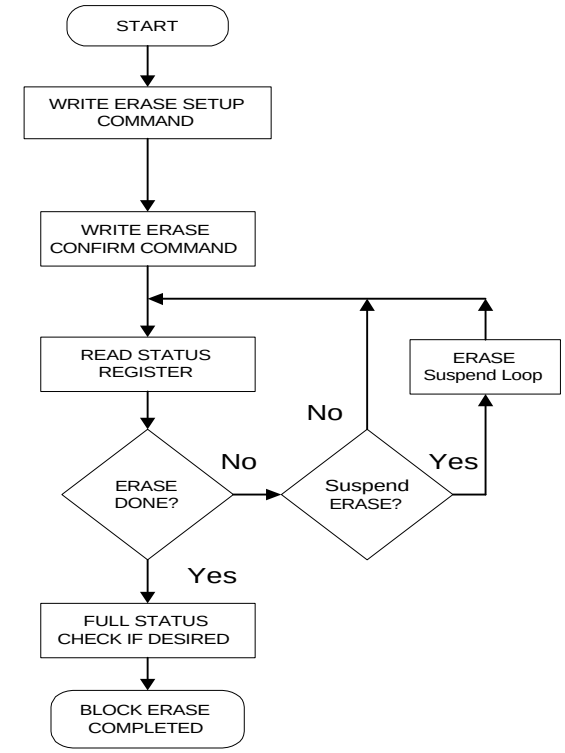
- The Host may monitor the Status Register 7 bit of each device to determine when an operation has completed.
- A single operation may be performed, then the appropriate device status register bits checked to determine if the operation completed successfully.
- Multiple operations may be performed, then the appropriate device status register bits checked to determine if all of the operation completed successfully.

Block Erase Suspend/Resume Commands :

The Block Erase Suspend command written to the WSM of a memory device allows block-erase interruption within that device in order to perform read or byte write operations in another block of memory. Writing the Block Erase Suspend command requests that the WSM of a device suspend the block erase sequence at a predetermined point in the algorithm. At this point, a Read Array command may be written to the device in order to read data from other blocks not involved in the erase operation. A Byte Write command sequence may also be issued during the erase suspend mode in order to program data in other memory blocks of a device. Block erase cannot resume until all write operations initiated during the block erase suspend period have been completed. In order to determine the status of the operation, a Read Status Register command may be written to a memory device (See Status Register Definitions Table).

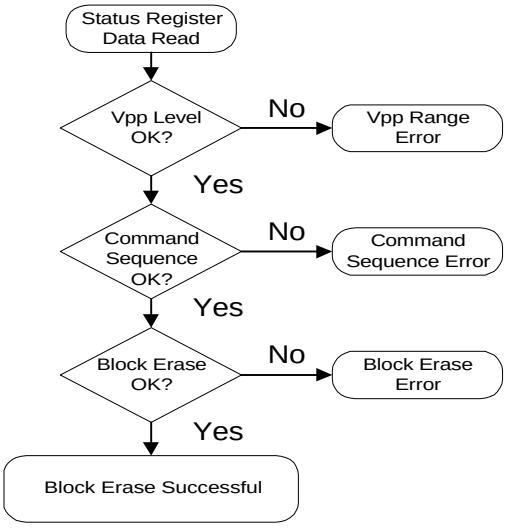
Writing a Block Erase Resume command to a device instructs the WSM of that device to resume performing any suspended block erase operations.

Block Erase Algorithm Description Table and Diagram :



Command	Bus	×8 Mode	×16 Mode
Erase Setup	Write	Data = 20h Address = Block	Data = 20h Address = Block Pair
Erase Confirm	Write	Data = D0h Address = Block	Data = D0D0h Address = Block Pair
Device Status Register Read	Read	Status Register Data update	Status Register Data update
	Standby	Check SR Bit 7 1 = Ready, 0 = Busy	Check SR Bit 7 and 15 1 = Ready, 0 = Busy

Full Status Check Procedure



Bus	×8 Mode	×16 Mode
Standby	Check SR Bit 3 1 = Vpp Detected Low	Check SR Bit 3 and 11 1 = Vpp Detected Low
Standby	Check SR Bit 4 and 5 All 1's = Command Sequence Error	Check SR Bit 4, 5, 12 and 13 All 1's = Command Sequence Error
Standby	Check SR Bit 5 1 = Block Erase Error	Check SR Bit 5 and 13 Both 1 = Block Erase Failure

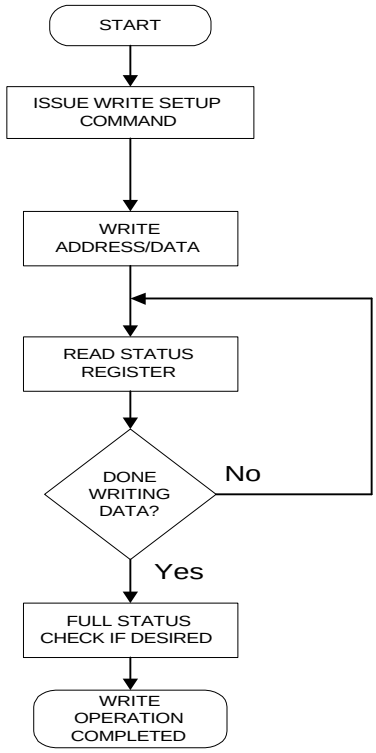
Byte Write Command :

The Byte Write Command is executed by a two-cycle command sequence written to the WSM of an individual memory device (See Command Definitions Table). Byte write operations are Write Enable controlled. The memory device latches address and data information on the rising edge of /WE (See CARD TIMING OPERATIONS). The WSM of each memory device controls the byte write and write verify algorithms and automatically updates the status register data of the device, freeing the Host of these tasks. The Host can detect completion of the operation by analyzing the status register SR7 data bit of that device. However, in order to determine if an operation has completed successfully without encountering any errors, the Status Register bits SR5, SR4, and SR3 of that device should also be checked (See Status Register Definitions Table).

A system designer has the following choices when initiating the Byte Write Command:

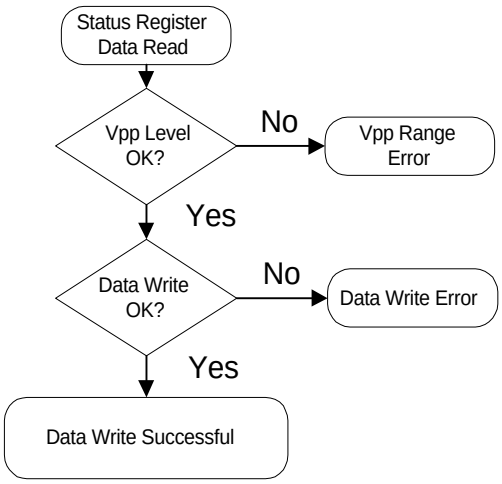
- The Host may monitor the Status Register 7 bit of each device to determine when an operation has completed.
- A single operation may be performed, then the appropriate device status register bits checked to determine if the operation completed successfully.
- Multiple operations may be performed, then the appropriate device status register bits checked to determine if all of the operation completed successfully.

Byte Write Algorithm Description Table and Flow Chart :



Command	Bus	×8 Mode	×16 Mode
Write Setup	Write	Data = 40h Address = Byte	Data = 40h Address = Word
Data Write	Data Write	Data to be written Address = Byte	Data to be written Address = Word
Device Status Register Read	Read	Status Register Data update	Status Register Data update
	Write	Check SR Bit 7 1 = Ready, 0 = Busy	Check SR Bit 7 and 15 1 = Ready, 0 = Busy

Full Status Check Procedure



Bus	×8 Mode	×16 Mode
Standby	Check SR Bit 3 1 = Vpp Detected Low	Check SR Bit 3 and 11 1 = Vpp Detected Low
Standby	Check SR Bit 4 1 = Data Write Error	Check SR Bit 4 and 12 1 = Data Write Error

Read Status Register Command :

The Status register of each device may be read to determine when a block erase or byte write operation is completed and whether the operation completed successfully (See Status Register Definitions Table). The Status Register Command may be written to a device whenever the device is ready to accept a new command. After which further read operations of the device will output data from the status register of that device until a different command is initiated. In order to update the status register of a device, /OE or /CE must toggle to a logic high value before status information is made current. The status register contents are latched by the device on the falling edge of /OE or /CE, whichever occurs first.

The Host system designer may chose to execute several repeated operations in one or several memory components before checking the Status Register of a given device. In this way the Host is able to execute several operation at once, and then determine if all of the operations completed successfully.

Clear Status Register Command :

Once Status Register bits SR5, SR4, and SR3 of a memory device have been set to "1"s by the WSM, indicating various failure conditions, only a Clear Status Register Command (50h) will resets all register bits of the device to "0" (See Status Register Definitions Table).

It is important to note that this command is not available during block erase or byte write suspend modes.

Status Register Definitions Table:

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
WSMS	ESS	ES	WBS	VPPS	R	R	R

Note: *These Status Register Bits are per memory device and are equivalent to output data bits [15:8] of the Odd byte of memory and bits [7:0] on the Even byte of memory.*

Field and Bit Values	Status Indications
WSMW = Write State Machine Status 1 = Ready 0 = Busy	Check RDY/BY or SR7 to determine block erase, byte write, completion.
ESS = Erase Suspend Status 1 = Block Erase Suspended 0 = Block Erase in Progress/Complete	Erase Suspend Status: SR6 may not equal "0" when SR7 equals "0"
ES = Erase Status 1 = Error in Block Erasure 0 = Successful of Block Eraser	If both SR5 and SR4 are "1"s after a block erase attempt, an improper command sequence was entered.
WBS = Program and Set Lock-Bit Status 1 = Error in Byte Write 0 = Successful Byte Write	If both SR5 and SR4 are "1"s after a block erase attempt, an improper command sequence was entered.
VPPS = Vpp Status 1 = Vpp Low Detected, Operation Abort 0 = Vpp OK	The WSM interrogates and indicates the Vpp level only after Block Erase, Byte Write command sequence.
R = Reserved for Future Enhancements	Reserved for Future use and should be masked out when polling the status register.

CARD TIMING CHARACTERISTICS

(Standard operating times for both Common and Attribute Memory unless otherwise noted.)

Read Cycle Timing (/WE = V_{HI})

Parameter	Symbol	Min	Max	Units
Read Cycle Time	t_{AVAV}	200		ns
Address Access Time	t_{AVQV}		200	ns
Card Enable Access Time	t_{ELQV}		200	ns
Output Enable Access Time	t_{GLQV}	125		ns
/OE High to Data Output Disable	t_{GHQZ}		90	ns
/CE Low to Data Output Enable	t_{ELQNZ}	5		ns
Address change to Data no longer valid	t_{AXQX}	0		ns
Address Setup to /OE Low time	t_{AVGL}	20		ns
/OE High Setup to Address time	t_{GHAX}	20		ns
/CE Low Setup to /OE Low time	t_{ELGL}	0		ns
/OE High to /CE High Hold time	t_{GHEH}	20		ns
Power (VCC) to High to Output Access Time	t_{PHQV}		400	ns

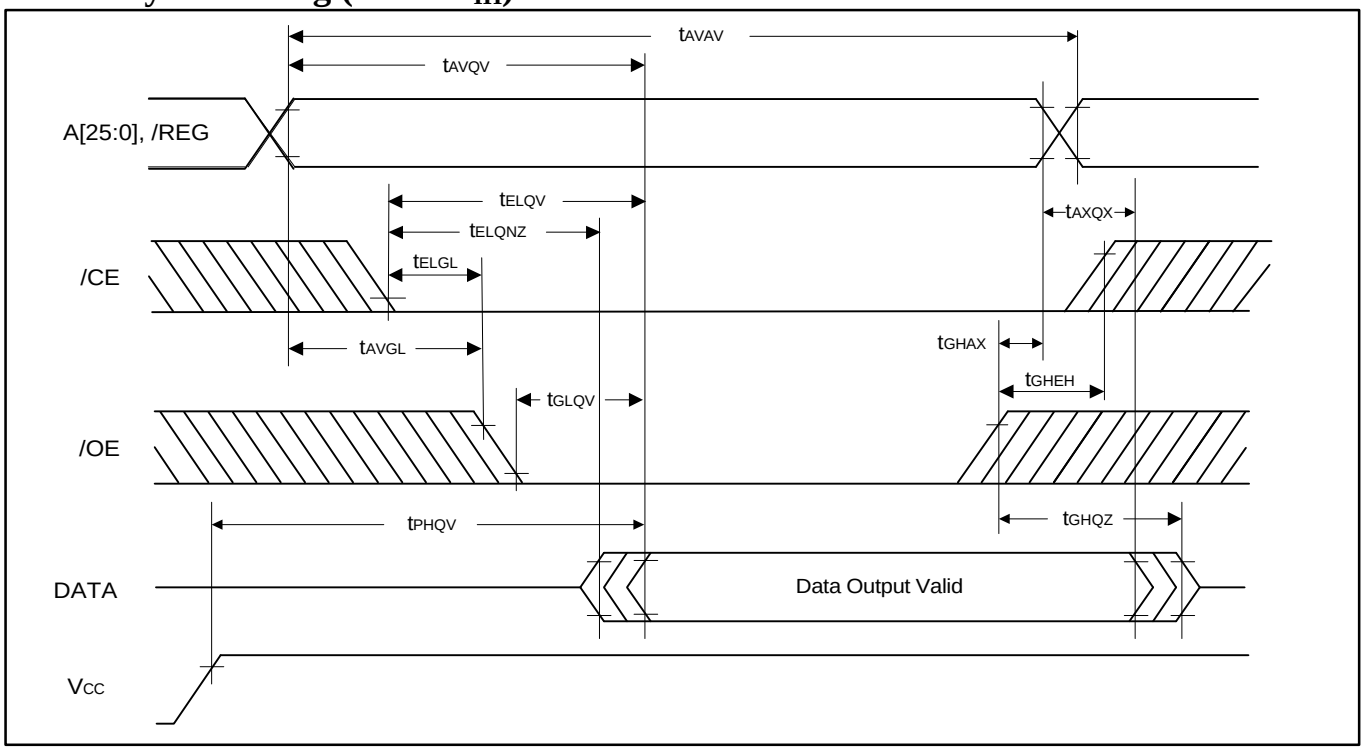
Write Cycle Timing (/OE = V_{HI})

Parameter	Symbol	Min	Max	Units
Write Cycle Time	t_{AVAV}	200		ns
Write Pulse Width	t_{WLWH}	120		ns
Address Setup Time for /WE Low	t_{AVWL}	20		ns
Address Setup to /WE High	t_{AVWH}		140	ns
Card Enable Setup to /WE Low	t_{ELWH}	140		ns
Data Setup to /WE High	t_{DVWH}	60		ns
Data Hold from /WE High	t_{WHDX}	30		ns
Address Hold from /WE High	t_{WHAX}	30		ns
Data Output Disable Time from /WE Low	t_{WLQZ}		90	ns
Data Output Disable Time from /OE Low	t_{GHQZ}		90	ns
/WE High time to Data Output Enable	t_{WHQNZ}	5		ns
/OE Low time to Data Output Enable	t_{GLQNZ}	5		ns
/OE High to /WE Low Setup time	t_{GHWL}	10		ns
/WE High to /OE Low Hold time	t_{WHGL}	10		ns
/CE Low to /WE Low Setup time	t_{ELWL}	0		ns
/WE High to /CE High Hold time	t_{WHEH}	20		ns

CARD TIMING CHARACTERISTICS *(CONTINUED)*

Common and Attribute Memory Read and Write Cycle Timing.

READ Cycle Timing (/WE=V_{IH})



CARD TIMING CHARACTERISTICS *(NOTE 1)* *(CONTINUED)*

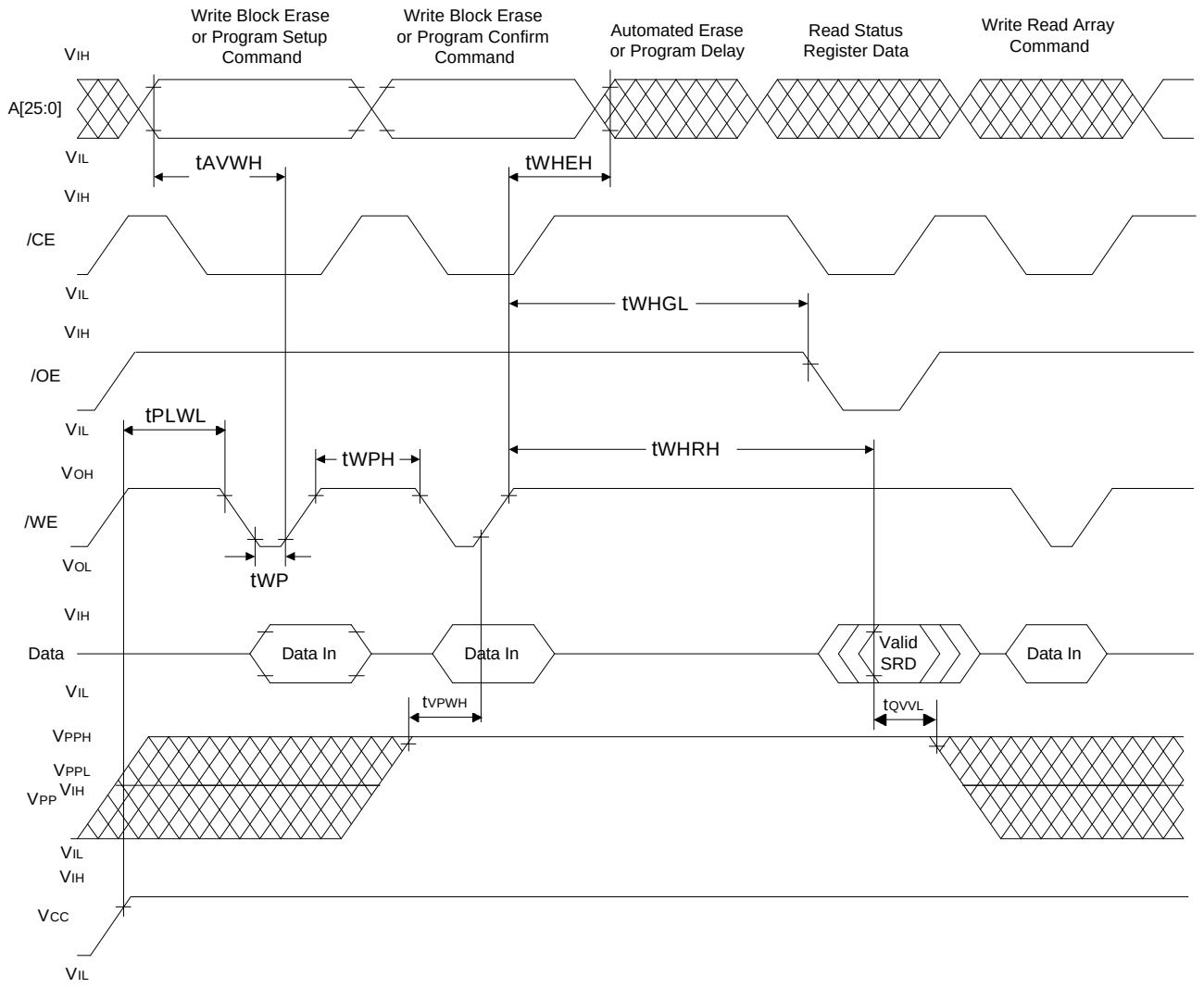
Memory component Timing Characteristics

Parameter	Symbol	**Min**	**Max**	**Unit**
Power (VCC) High Recovery to /WE Going Low	t_{PHWL}	1		µs
Address Setup to /WE Going High	t_{AVWH}	40		ns
/CE (/WE) Hold from /WE High	t_{WHEH}	10		ns
Address Hold from /WE High	t_{WHDX}	5		ns
Write Pulse Width	t_{WP}	50		ns
Write Pulse Width High	t_{WPH}	30		ns
Write Recovery before Read	t_{WHGL}	0		ns
V_{PP} Setup to /WE going Low	t_{VPWH}	100		ns
V_{PP} Hold from Valid SRD	t_{QVVL}	0		ns

Notes:

1. *Read Timing characteristics during Block Erase Suspend operations are the same as during read operations. Refer to AC Characteristics for read operations.*

COMMON MEMORY PROGRAM/ERASE TIMING DIAGRAM

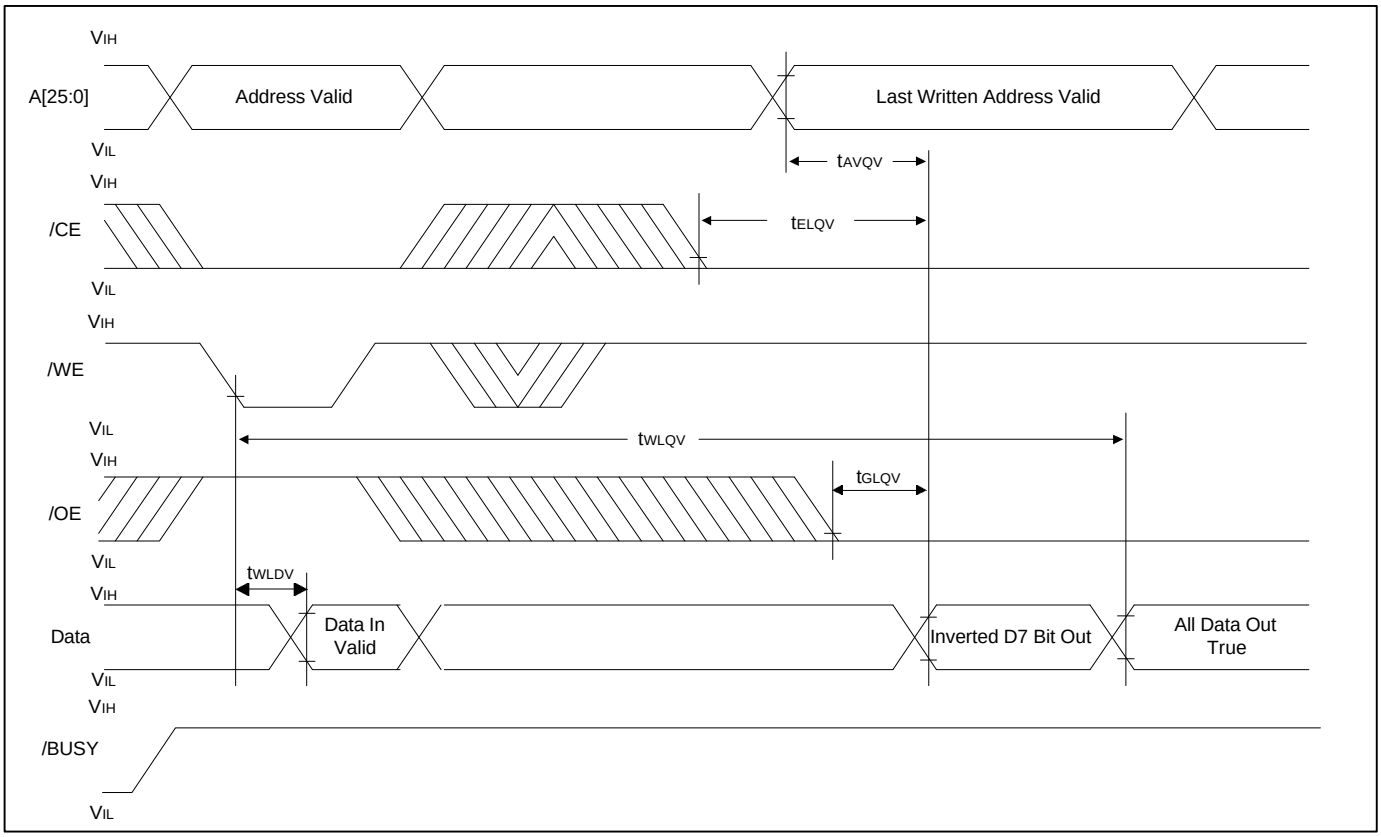


Operation Mode (Note1)	Symbol	Min	Max	Unit
Program Time	t_{WHRH}	6.5		µs
Block Erase		0.9		sec

Note:

1. Maximum values are To Be Determined. (TBD).

ATTRIBUTE MEMORY TIMING DIAGRAM



Attribute Parameter **(Note 1, 2)**	Symbol	**Min**	**Max**	**Unit**
Read Cycle Time	t_{AVAV}	200		ns
Card Enable Access Time	t_{ELQV}		200	ns
Output Enable Access Time	t_{GLQV}		70	ns
Write Enable Low to Data Valid Time	t_{WLDV}		1000	ns
Write Enable Low to Data Read Valid Time	t_{WLQV}		1	ms

Note:

1. *All timing values are constant with standard Read/Write Times, unless otherwise shown in the Table.*
2. *Attribute memory latches address values on the falling edge of /WE. Data is latched on the rising edge of /WE.*

Attribute Data Polling Mode :

Data Polling the 28C16A features /DATA polling to signal the completion of a byte write cycle. During a write cycle, an attempt to read the last byte written to memory will produce the complement of the D7 (D6 to D0 are indeterminate). After completion the true data is available. Data Polling allows a simple read/compare operation to determine the status of the chip.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-40ºC to +85ºC
Operating Temperature with Power Applied	0ºC to +70ºC
Voltage on Any Pin (except V_{CC} and V_{PP})	-2.0 V to +7.0 V
V_{PP} Program Voltage	-2.0 V to +14.0 V
V_{CC} Supply Voltage	-2.0 V to +7.0 V

Cards are not guaranteed to function at Absolute Maximum Ratings and are not intended to be exposed to these conditions for extended periods of time. Long term exposure may damage these cards or adversely effect the card reliability.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min.	Max.	Units
Vcc Supply Voltage	Vcc	4.75	5.25	V
V_{PPH} Programming Voltage High	V_{PPH}	11.40	12.60	V
V_{PPL} Programming Voltage Low	V_{PPL}	0.0	6.5	V
Operating Temperature	T_A	0	70	°C

DC CHARACTERISTICS

Supply current is an RMS value. Typical values at nominal V_{CC} voltage at T_A = +25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CCS}	Standby Current **(Notes 2)**	Per device CMOS; $V_{CC} = V_{CC}$ Max /CE1, /CE2, = V_{CC} ±0.2V		50	150	µA
I_{CCR}	Active Read Current **(Note 1, 2)**	CMOS; $V_{CC} = V_{CC}$ Max /CE1 or /CE2 = GND **Byte (×8)** f = 8MHZ, I_{OUT} = 0mA		20	35	mA
		Byte (×16)		40	70	mA
I_{CCW}	Active Program Current **(Note 1, 3)**	Per device (including programming current)			75	mA
I_{CCE}	Active Block Erase Current **(Note 3)**	Per device (including programming current)			50	mA
I_{CCWS} I_{CCES}	Program Suspend or Block Erase Suspend Current	Per device /CE1, /CE2 = V_{IH}		1	10	mA
I_{IL}	Input Leakage Current	V_{IN} = GND to V_{CC}, $V_{CC\ MAX}$ Per Pin			±20	µA
I_{ILpu}	Input Leakage Current with Pull Up Resistor	V_{IN} = GND to V_{CC}, $V_{CC\ MAX}$ Per Pin with 10KΩ pull up resistor			+500	µA
I_{ILpd}	Input Leakage Current with Pull Down Resistor	V_{IN} = GND to V_{CC}, $V_{CC\ MAX}$ Per Pin with 100KΩ pull down resistor			-50	µA
I_{OLpd}	Output Leakage Current with Pull Down Resistor	V_{IN} = GND to V_{CC}, $V_{CC\ MAX}$ Per Pin with 100KΩ pull down resistor			-50	µA
V_{IL}	Input Low Voltage **(Note 3)**		-0.5		0.8	V
V_{IH}	Input High Voltage **(Note 3)**		$0.7 \times V_{CC}$		V_{CC} +0.5	V
V_{OL}	Output Low Voltage **(Notes 3)**	$V_{CC} = V_{CC}$ Min I_{OL} = 2 mA (3.3V) = 5.8 mA (5V)			0.45	V
V_{OH}	Output High Voltage **(Notes 3)**	CMOS; $V_{CC} = V_{CC}$ Min I_{out} = -2.5mA	$0.85 \times V_{CC}$			V
		CMOS; $V_{CC} = V_{CC}$ Min I_{out} = -100µA	V_{CC} -0.4			V

Notes:

1. *I_{CCWS} and I_{CCES} are specified with the device deselected. If read or written while in erase suspend mode, the device's current is the sum of I_{CCWS} or I_{CCWS} and I_{CCR} or I_{CCW}.*
2. *CMOS inputs are either VCC ± 0.2V or GND ± 0.2V.*
3. *Sample tested by component manufacturer.*

CARD INFORMATION STRUCTURE

The CIS is data which describes the PCMCIA card and is described by the PCMCIA standard. This information can be used by the Host system to determine a number of things about the card that has been inserted. For information regarding the exact nature of this data, and how to design Host software to interpret it, refer to the PCMCIA standard Metaformat Specification.

Physical Address	Logical Address	Data Value(s)	Tuple Description
00h	00h	01h	CISTPL_DEVICE
02h	01h	03h	CISTPL_LINK
04h	02h	52h	Speed = 200ns, WPS=Yes, FLASH
06h	03h	**4Eh** ***(Note 1)***	Bits 2-0 = 110b = 2 Meg units, Bits 7-3 = 01001b = 10 Units (0=1, 1=2...) 2 Meg x 10 = 20 Meg size
08h	04h	FFh	CISTPL_END - End of Tuple
0Ah	05h	18h	CISTPL_JEDEC
0Ch	06h	03h	CISTPL_LINK
0Eh	07h	89h	Manufacturer ID (Intel)
10h	08h	A2h	Device ID (28F008SA)
12h	09h	FFh	CISTPL_END - End of Tuple
14h	0Ah	1Eh	CISTPL_DEVICEGEO
16h	0Bh	07h	CISTPL_LINK
18h	0Ch	02h	DGTPL_BUS - Bus Width - 2 Bytes
1Ah	0Dh	11h	DGTPL_EBS - Erase Block Size 2^10h = 64K Bytes or Words
1Ch	0Eh	01h	DGTPL_RBS - Byte Accessible
1Eh	0Fh	01h	DGTPL_WBS - Byte Accessible
20h	10h	01h	DGTPL_PART - One Partition
22h	11h	01h	DGTPL_HWIL - No Interleave
24h	12h	FFh	CISTPL_END - End of Tuple

Note:

1. *Refer to the table (right) for capacity of the card and corresponding data value.*

Capacity	Data value
02MB	06h
04MB	0Eh
06MB	16h
08MB	1Eh
10MB	26h
12MB	2Eh
14MB	36h
16MB	3Eh
18MB	46h
20MB	4Eh

Notes continued next page.

CARD INFORMATION STRUCTURE *(CONTINUED*

Physical Address	Logical Address	Data Value(s)	Tuple Description
26h	13h	15h	CISTPL_VERS1
28h	14h	**58h** ***(Note 2)***	CISTPL_LINK
2Ah	15h	04h	TPLLV1_MAJOR (PCMCIA 2.1/JEIDA 4.2)
2Ch	16h	01h	TPLLV1_MINOR
2Eh...66h	17h...33h	43 65 6E 74 65 6E 6E 69 61 6C 20 54 65 63 68 6E 6F 6C 6F 67 69 65 73 2C 20 49 6E 63 2E	ASCII Text is : Centennial Technologies, Inc. {29 Characters total}
68h	34h	00	NULL String Delimiter (String 1)
6Ah...84h	35h...42h	46 4C 32 30 4D 2D 32 30 2D 31 31 31 33 38	ASCII Text is : ***(Note 3)*** **FL20M-20-11138** {16 Characters total}
86h	43h	00	NULL String Delimiter (String 2)
88h...CAh	44h...65h	32 30 20 4D 45 47 20 46 4C 41 53 48 20 77 2F 38 20 4D 62 69 74 20 49 6E 74 65 6C 20 64 65 76 69 63 65 73	ASCII Text is : ***(Note 4)*** **20 MEG FLASH w/8 Mbit Intel devices** {35 Characters total}
CCh	66h	00	NULL String Delimiter (String 3)
CEh	67h	00	NULL String Delimiter (String 4)
D0h	68h	FF	CISTPL_END - End of Tuple

D2h	69h	FF	CISTPL_END - End of Chain Tuple

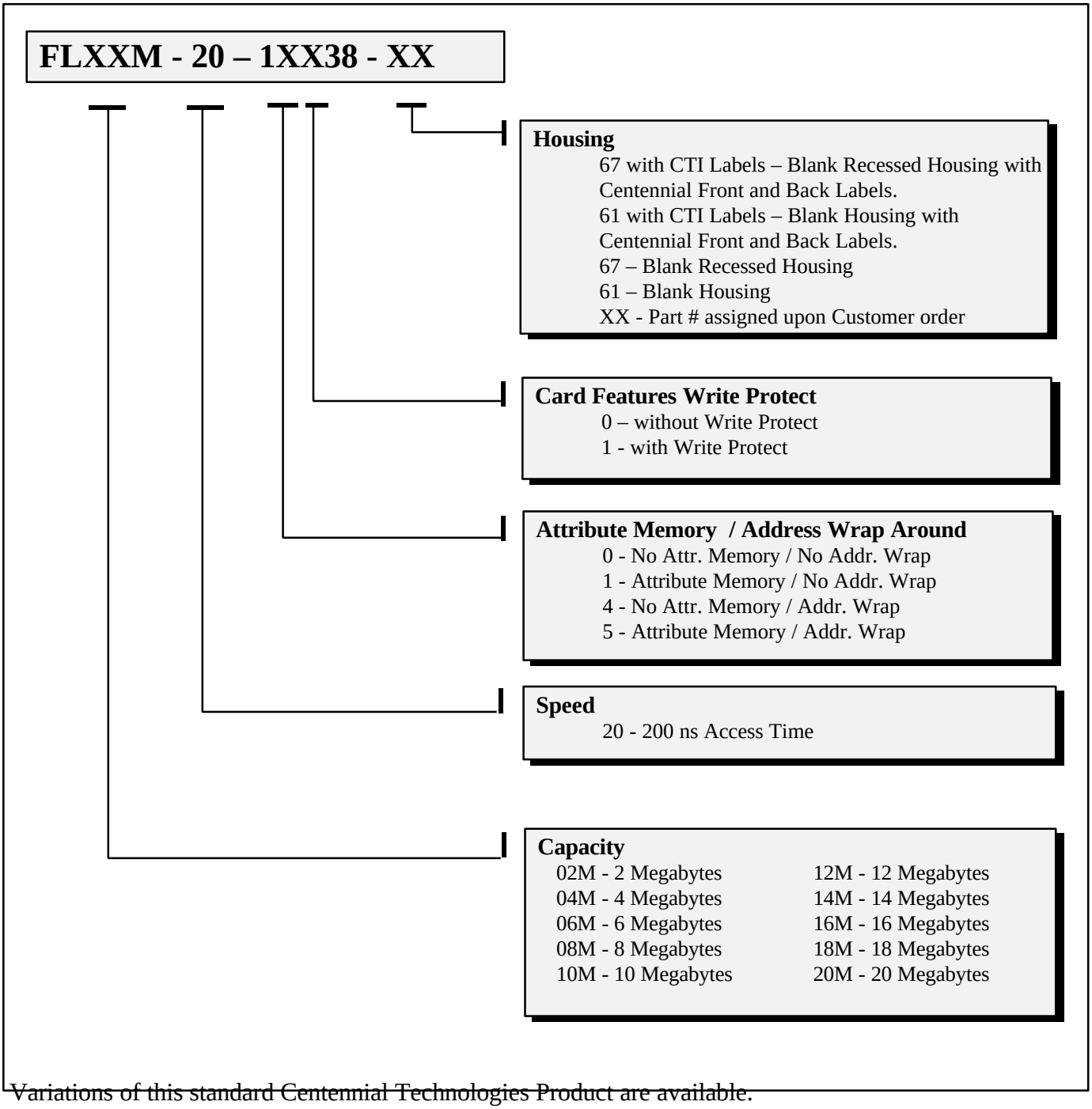
Notes:

2. *Products with memory capacities of less than two digits will have a Data Value of 57h. All address values will be adjusted accordingly.*
3. *Specific Product description will be listed.*
4. *Specific Product memory capacities will be listed for specific products.*

SALES AND SUPPORT

To order or to obtain information on pricing or delivery, contact a Centennial Technologies Sales and Support representative.

PART NUMBER INFORMATION



Variations of this standard Centennial Technologies Product are available.
Contact a Centennial Sales Representative for additional information.